Mobile Files

Special Thanks!

130877
TRALOL
weaver
wins200786
QueenSoft
Mihail_tm
abraziff

iPad 2

Professional Schematic!

A1395,A1396,A1397(k94ap)

Wites OM Tesla





GSM-FORUM

Special Thanks!

..::Neo::..
~AhmedLeO~
Gecko UK
Mobileinfo
Hobson
Noobfix
DataRus
Kostelectronics
diesel57

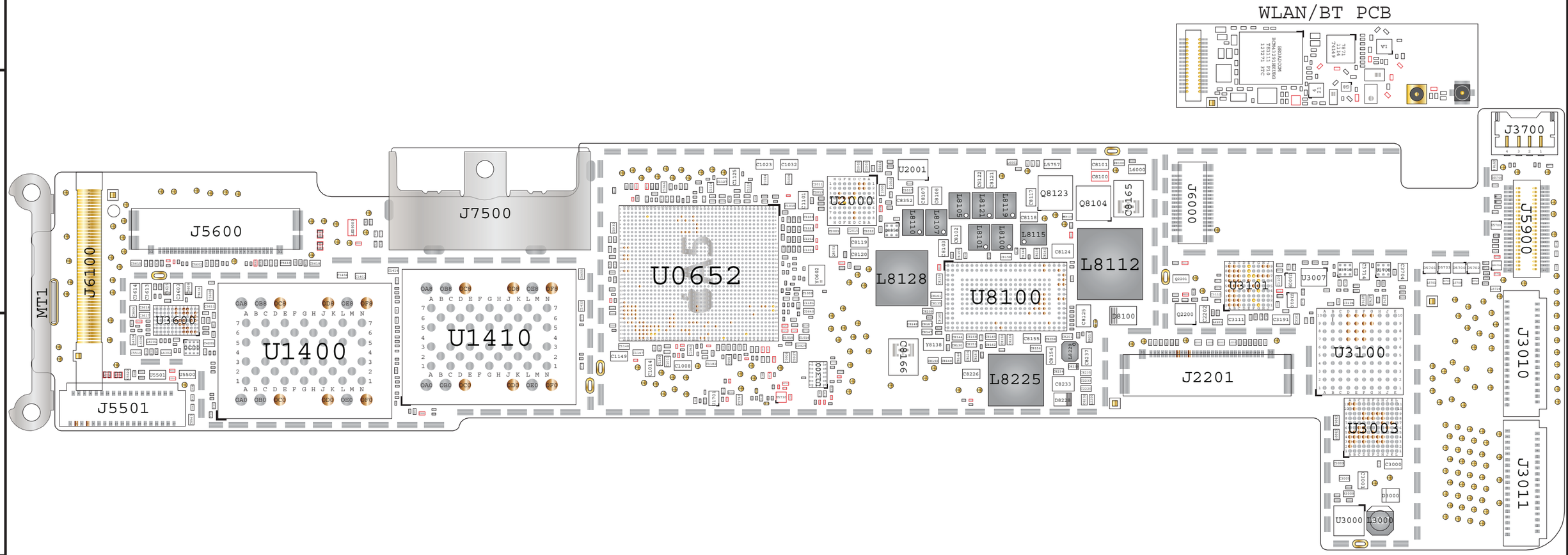
Wites OM Tesla
READ BEFORE PROCEED!

PRINTS MARKED WITH COPER ARE NC,EMPTY!

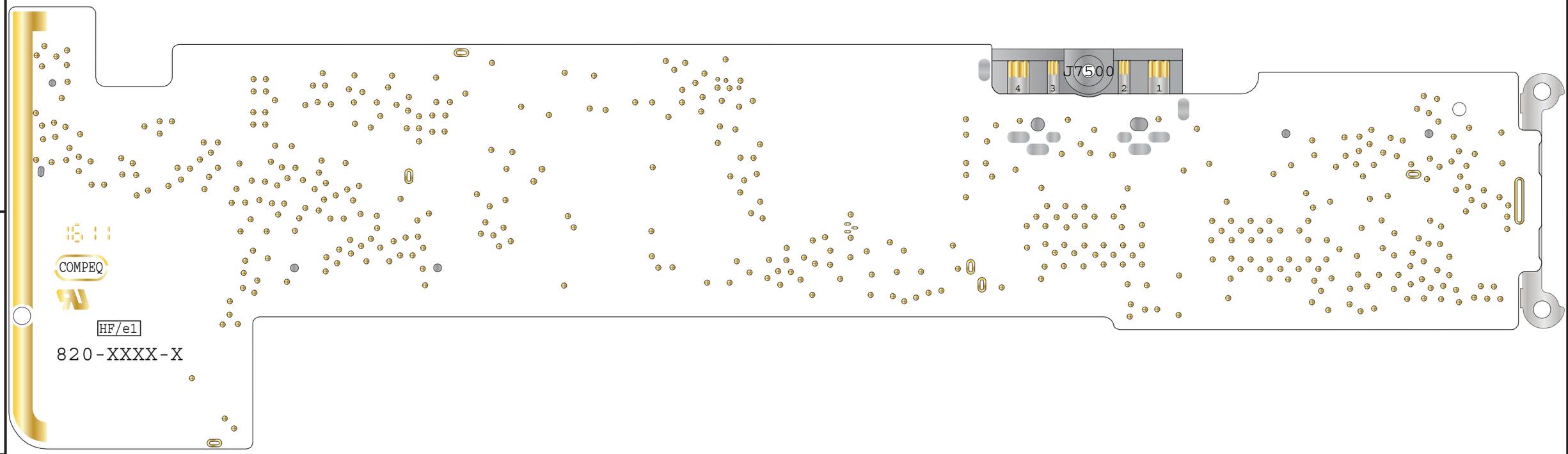
PRINTS MARKED WITH GOLD ARE CONNECTED ONLY TO TEST POINTS NO OTHER CIRCUIT!

IF YOU REBALL U3100 LOOK CAREFUL IF B9 AND B10 THAT LOOK LIKE A JUMPER IS REMOVED TOUCH WILL NOT WORK IF SO HAPPEN MAKE A JUMPER ON THE IC!

NOSTUFF COMPONENTS JUST LOOK ON BOARD THEY ARE NOT MOUNTED(MISSING)!



820-2875-05 MLB TOP PCB



820-2875-05 MLB BOTTOM PCB

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K94 CHOPIN MLB

PVT

REV. A

LAST_MODIFIED=Mon Jan 10 13:11:06 2011

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0001052699	PRODUCTION RELEASED	2011-01-10

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	TABLE OF CONTENTS	MIKE	N/A
2	2	BLOCK DIAGRAM: SYSTEM	MIKE	N/A
3	5	BOM TABLE	MIKE	N/A
4	6	AP: MAIN	JAMES	N/A
5	7	AP: I/Os	JAMES	N/A
6	8	AP: NAND	JAMES	N/A
7	9	AP: TV,DP,MIPI	JAMES	N/A
8	10	AP: PWR	JAMES	N/A
9	11	AP: PWR	JAMES	N/A
10	12	AP: MISC & ALIASES	JAMES	N/A
11	13	AP: VIDEO BUFFER,BB USB MUXES	JAMES	N/A
12	14	NAND	JONATHAN	N/A
13	17	VIDEO: DISPLAY PORT	JAMES	N/A
14	20	VIDEO: MLC	MIKE	N/A
15	21	VIDEO: MLC ALIASES	MIKE	N/A
16	22	VIDEO: LVDS CONNECTOR	ALEX	N/A
17	30	GRAPE: GROUNDHOG,CONN,BOOST	RAMSIN	N/A
18	31	GRAPE: Z1, Z2	RAMSIN	N/A
19	36	AUDIO: L63 CODEC	LENG	N/A
20	37	AUDIO: SPEAKER AMP	LENG	N/A
21	38	AUDIO: HEADPHONE OUT	LENG	N/A
22	39	AUDIO: BLANK	LENG	N/A
23	42	AUDIO: DETECT/MIC BIAS	LENG	N/A
24	43	AUDIO: HP/MIC FILTERS	LENG	N/A
25	54	CONNECTOR: CANADA FLEX CONN,SENSOR PANEL ALIASES	MARK B.	N/A
26	55	CONNECTOR: CANADA FLEX FILTERS	MARK B.	N/A
27	56	CONNECTOR: SENSOR PANEL CONNECTOR	MARK B.	N/A
28	57	IO FLEX: DOCK COMPONENTS	JAMES	N/A
29	59	IO FELX: B2B Connector	JAMES	N/A
30	60	CONNECTOR: X23 WIFI/BT	MIKE	N/A
31	61	CONNECTOR: X24 CELLULAR/GPS	MIKE	N/A
32	73	POWER: ALIASES	YOSH	N/A
33	75	POWER: BATTERY CONNECTOR	YOSH	N/A
34	81	POWER: PMU	YOSH	N/A
35	82	POWER: PMU	YOSH	N/A
36	83	POWER: 3.3V VR	YOSH	N/A
37	90	DEBUG AND MISC	MIKE	N/A
38	93	FCT/ICT TEST/BRACKETS	MIKE	N/A
39	100	CONSTRAINTS: ASSIGNMENTS	MIKE	N/A
40	101	CONSTRAINTS: ASSIGNMENTS	MIKE	N/A
41	102	CONSTRAINTS: MLB RULES	MIKE	N/A
42	106	CONSTRAINTS: RF RULES	MIKE	N/A

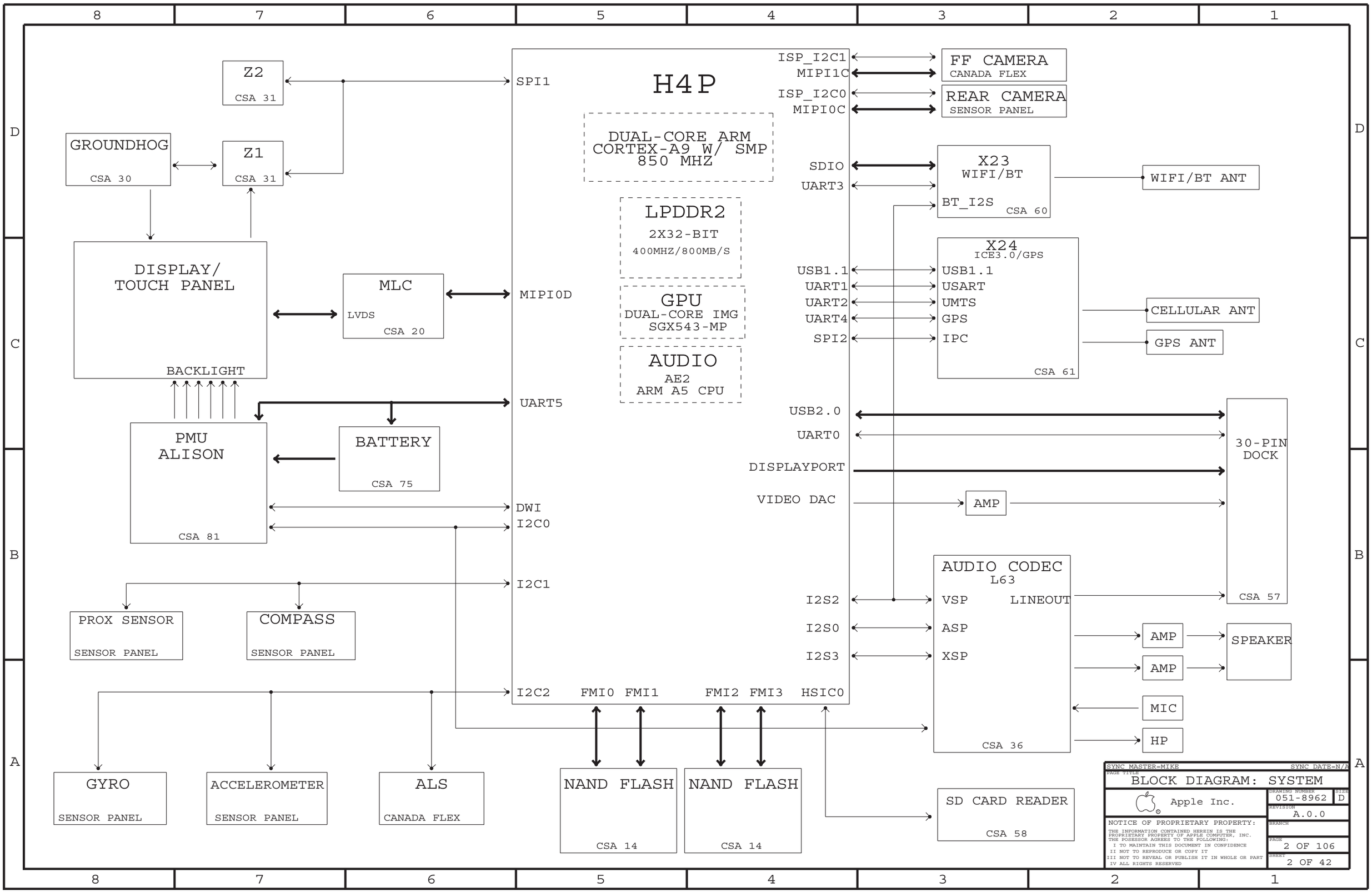
_DRAWING
TITLE=BACH
ABBREV=DRAWING

DRAWING TITLE: CHOPIN MLB

Apple Inc.

DRAWING NUMBER: 051-8962 | SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 1 OF 106
SHEET: 1 OF 42

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC MASTER=MIKE SYNC DATE=N/A

PAGE TITLE

BLOCK DIAGRAM: SYSTEM

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

BRANCH

PAGE 2 OF 106

SHEET 2 OF 42

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

IV ALL RIGHTS RESERVED

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

ALL AVAIL BOM OPTIONS

COMMON
ALTERNATE

16GB_PROD
32GB_PROD
64GB_PROD

BKLT_PLL

DEVELOPMENT_JTAG
DEVELOPMENT_JTAG_TAP
JTAG_DAP
JTAG_TAP_NOT

SPEAKER
INTERNAL_MIC

PORTRAIT_DOCK

MLC_DEV
MLC_PROD

K93
K94

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE

ADD DEVELOPMENT AND OTHER BOMS ONCE YOU GET BOM NUMBERS

BOM OPTIONS

PROGRAMMABLE PARTS

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-8962	1	SCH,CHOPIN_AUDIO,MLB,K94	SCH1	
820-3069	1	PCBF,CHOPIN_AUDIO,MLB,K94	PCB1	

PD PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
806-1396	1	FENCE,GRAPE,MLB,K93/K94	FENCE1	
806-1397	1	CAN,GRAPE,MLB,K93/K94	CAN1	NOSTUFF
806-1398	1	FENCE,CPU,MLB,K93/K94	FENCE2	
806-1399	1	CAN,CPU,MLB,K93/K94	CAN2	NOSTUFF
806-1400	1	FENCE,NAND,MLB,K93/K94	FENCE3	
806-1401	1	CAN,NAND,MLB,K93/K94	CAN3	NOSTUFF

TOP BARCODE LABEL/EEE CODES
(ONLY ONE IS USED PER BOM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7651	1	EEEE FOR 639-1180 (K93 16G)	DH36	CRITICAL	EEEE_K93_16G
825-7651	1	EEEE FOR 639-1426 (K93 32G)	DH37	CRITICAL	EEEE_K93_32G
825-7651	1	EEEE FOR 639-1428 (K93 64G)	DG99	CRITICAL	EEEE_K93_64G
825-7651	1	EEEE FOR 639-1112 (K94 16G)	DFC4	CRITICAL	EEEE_K94_16G
825-7651	1	EEEE FOR 639-1181 (K94 32G)	DFC5	CRITICAL	EEEE_K94_32G
825-7651	1	EEEE FOR 639-1182 (K94 64G)	DFC6	CRITICAL	EEEE_K94_64G
825-7651	1	EEEE FOR 639-1430 (K95 16G)	DH3C	CRITICAL	EEEE_K95_16G
825-7651	1	EEEE FOR 639-1427 (K95 32G)	DH3D	CRITICAL	EEEE_K95_32G
825-7651	1	EEEE FOR 639-1429 (K95 64G)	DG9C	CRITICAL	EEEE_K95_64G

BOTTOM LABEL TYPE 1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7639	1	631- B/C LABEL	LBL1	CRITICAL	
825-7639	1	639- B/C LABEL	LBL2	CRITICAL	

BOTTOM LABEL TYPE 2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7640	1	MATRIX LABEL	LBL3	CRITICAL	
825-7640	1	631- MATRIX LABEL	LBL4	CRITICAL	

SYNC MASTER=MIKE SYNC DATE=N/A

PAGE TITLE
BOM TABLE

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
PAGE 5 OF 106
SHEET 3 OF 42

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:

NEED TO ADD BOM TABLE FOR ALT P/N OF HYNIX (?)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION

U0652
H4P-512MB
BGA
SYM 11 OF 12
SC58940X01-A030

AU14 AU15 AU16 AU17 AV1 AV2 AV3 AV4 AV5 AV6 AV7 AV8 AV9 AV10 AV11 AV12 AV13 AV14 AV15 AV16 AV17 AV29 AV33 AV34 AW1 AW2 AW4 AW23 AW33 AW34 AY1 AY2 AY3 AY4 AY20 AY22 AY24 AY30 AY31 AY32 AY33 AY34 B1 B2 B7 B9 B10 B12 B13 B15 B17 B18 B20 B22 B23 B28 B30 B32 B33 B34 C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C23 C27 C29 C32 C33 D1 D3 D5 D7 D9 D11 D13 D15 D16 D23 — VSS

D27 D32 E1 E2 E3 E4 E6 E8 E10 E12 E14 E16 E17 E18 E19 E20 E21 E22 E23 E25 E26 E27 E28 E30 E31 E32 E34 F1 F2 F3 F5 F19 F20 F21 F22 F23 F25 F26 F29 F30 F31 F32 G1 G3 G4 G7 G8 G9 G10 G12 G13 G14 G15 G16 G17 G18 G19 G20 G21 G22 G25 G28 G29 G30 H1 H2 H3 H5 H7 H8 H10 H12 H14 H16 H18 H20 H22 H24 H25 H29 H30 J1 J2 J3 J4 J7 J9 J11 J13 J15 J17 J19 — VSS

=PP1V1_PLL_H4 → R0620 0.00 0% 1/32W MF 01005 → PP1V1_PLL4_F
- C0651 0.01UF 10% 6.3V X5R 01005
- VOLTAGE=1.1V; MIN_LINE_WIDTH=0.2MM; MIN_NECK_WIDTH=0.1MM; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM

R0621 0.00 → PP1V1_PLL3_F
- C0648 0.01UF 10% 6.3V X5R 01005
- VOLTAGE=1.1V; MIN_LINE_WIDTH=0.2MM; MIN_NECK_WIDTH=0.1MM; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM

R0622 0.00 → PP1V1_PLL2_F
- C0646 0.01UF 10% 6.3V X5R 01005
- VOLTAGE=1.1V; MIN_LINE_WIDTH=0.2MM; MIN_NECK_WIDTH=0.1MM; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM

R0623 0.00 → PP1V1_PLL1_F
- C0644 0.01UF 10% 6.3V X5R 01005
- VOLTAGE=1.1V; MIN_LINE_WIDTH=0.2MM; MIN_NECK_WIDTH=0.1MM; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM

R0624 0.00 → PP1V1_PLL0_F
- C0608 0.01UF 10% 6.3V X5R 01005
- C0660 56PF 5% 6.3V NPO-COG 01005
- VOLTAGE=1.1V; MIN_LINE_WIDTH=0.2MM; MIN_NECK_WIDTH=0.1MM; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM

JTAGSEL
0 - PARALLEL
1 - DAISY-CHAIN (FOR USE WITH 5-WIRE JTAG)
PER RADAR #6755237

=PP1V1_USB_H4 → C0643 0.22UF 20% 6.3V X5R 0201

=PP1V2_HSIC_H4 → C0642 0.01UF 10% 6.3V X5R 01005; C0641 0.01UF 10% 6.3V X5R 01005

HSIC_VDD121 D25 — 17MA
HSIC_VDD122 D24 — 17MA
HSIC_DVDD F24 — 7MA
PLL0_AVDD11 C19 — 2.5MA EACH
PLL1_AVDD11 C20
PLL2_AVDD11 C25
PLL3_AVDD11 C24
PLL4_AVDD11 C18
PLL_USB_AVDD11 C17 — 2.5MA
MIPI0D_VDD11_PLL AR20 — 6.5MA
MIPI1D_VDD11_PLL AT14
USB_DVDD C28 — 5MA
H27
USB_VDD330 M28 — 28MA

=PP1V1_USB_H4 → R0625 0.00 0% 1/32W MF 01005 → C0652 0.01UF 10% 6.3V X5R 01005

VOLTAGE=1.1V; MIN_LINE_WIDTH=0.2MM; MIN_NECK_WIDTH=0.1MM; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM
PP1V1_MIPID_PLL_F → FL0610 80-OHM-0.2A-0.4-OHM 0201-1 → =PP1V1_MIPI_PLL_H4
- C0661 56PF 5% 6.3V NPO-COG 01005
- C0654 0.1UF 10% 6.3V X5R 201
- C0655 1UF 10% 6.3V CERM 402

=PP1V1_USB_H4 → C0627 0.01UF 10% 6.3V X5R 01005

=PP3V3_USB_H4 → C0640 1UF 10% 6.3V CERM 402; C0630 0.01UF 10% 6.3V X5R 01005

=PP1V8_H4 → R0645 100K; R0646 100K; R0647 100K → JTAG_AP_TCK, JTAG_AP_TMS, JTAG_AP_TDI

DEVELOPMENT_JTAG_TAP → R0662 100K → AP_JTAG_SEL

=PP3V3_USB_H4 → R0617 10K 1% 1/32W MF 01005 → RST_AP_L

R0632 100K 1% 1/32W MF 01005 → NOSTUFF XW0604 SHORT-01005 → RST_AP_1V8_L

R0688 42.2K 1% 1/32W MF 01005 → C0618 1000PF 10% 16V X7R 201 → AP_CFSB

NOSTUFF XW0605 SHORT-01005 → AP_DDR1_CKEIN_1V2 → AP_DDR1_CKEIN

R0689 82.5K 1% 1/32W MF 01005

TP_HSIC1_AP_DATA	A26	HSIC1_DATA	
TP_HSIC1_AP_STB	A27	HSIC1_STB	
NC_HSIC2_AP_DATA	C26	HSIC2_DATA	
NC_HSIC2_AP_STB	D26	HSIC2_STB	
AP_JTAG_SEL	N31	JTAG_SEL	
NC_JTAG_AP_RTCK	M30	JTAG_TRTCK	
JTAG_AP_TRST_L	N29	JTAG_TRST*	
JTAG_AP_TDO	M31	JTAG_TDO	
JTAG_AP_TDI	M32	JTAG_TDI	
JTAG_AP_TMS	N32	JTAG_TMS	
JTAG_AP_TCK	N30	JTAG_TCK	
AP_TESTMODE	P29	TESTMODE	
	M28	FUSE1_FSRC	
AP_TST_STPCLK	P33	TST_STPCLK	
TP_AP_TST_CLKOUT	P34	TST_CLKOUT	
AP_FAST_SCAN_CLK	T32	FAST_SCAN_CLK (FOR IC TESTER)	
AP_HOLD_RESET	P31	HOLD_RESET (0=NORMAL)	
RST_AP_1V8_L	P32	RESET*	
AP_CFSB	W30	CFSB	
	G11	DDR0_CKEIN	
AP_DDR1_CKEIN	R7	DDR1_CKEIN	

SYM 1 OF 12
U0652
H4P-512MB
BGA

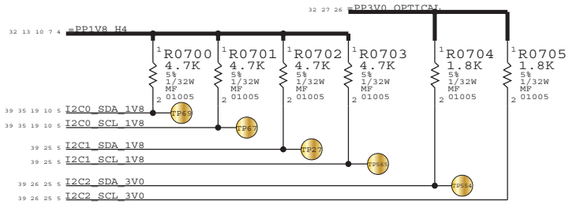
HSIC_VSS121 C25 — HSIC_VSS122 C24 — HSIC_DVSS E24 — PLL0_AVSS11 D19 — PLL1_AVSS11 D20 — PLL2_AVSS11 D21 — PLL3_AVSS11 D18 — PLL4_AVSS11 D17 — PLL_USB_AVSS11 D22 — MIPI_VSS_0 AN10 — MIPI_VSS_1 AN11 — USB_DVSS D28 — USB_VSSA0 H26 — USB_VSSAC J26

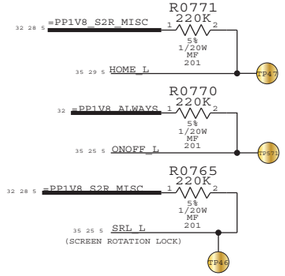
	P30	WDOG	RST_PMU_IN → PMU
XTAL_24M_I	A18	XI0	R0655 1.00M 1% MF 01051/32W
XTAL_24M_O	A19	XO0	R0640 22 5% 1/32W MF 01005 → CRITICAL Y0602 SM-2 24.000MHZ-16PF-60PPM; C0613 22PF 5% 16V CERM 01005; C0607 22PF 5% 16V CERM 01005
USB_FS_D_P	A22	USB11_DP	
USB_FS_D_N	A23	USB11_DM	
USB_D_P	A29	USB_DP	
USB_D_N	A28	USB_DM	
NC_USB_ANALOGTEST	G26	USB_ANALOGTEST	
USB_AP_VBUS	F27	USB_VBUS	R0651 100K 5% 1/32W MF 01005 → PPVBUS_USB; DZ0600 GDZT2R5.1B GDZ-0201
NC_USB_ID	F28	USB_ID	
	G27	USB_BRICKID	→ USB_BRICKID → PMU
USB_REXT	A21	USB_REXT	R0642 44.2 1% 1/20W MF 201

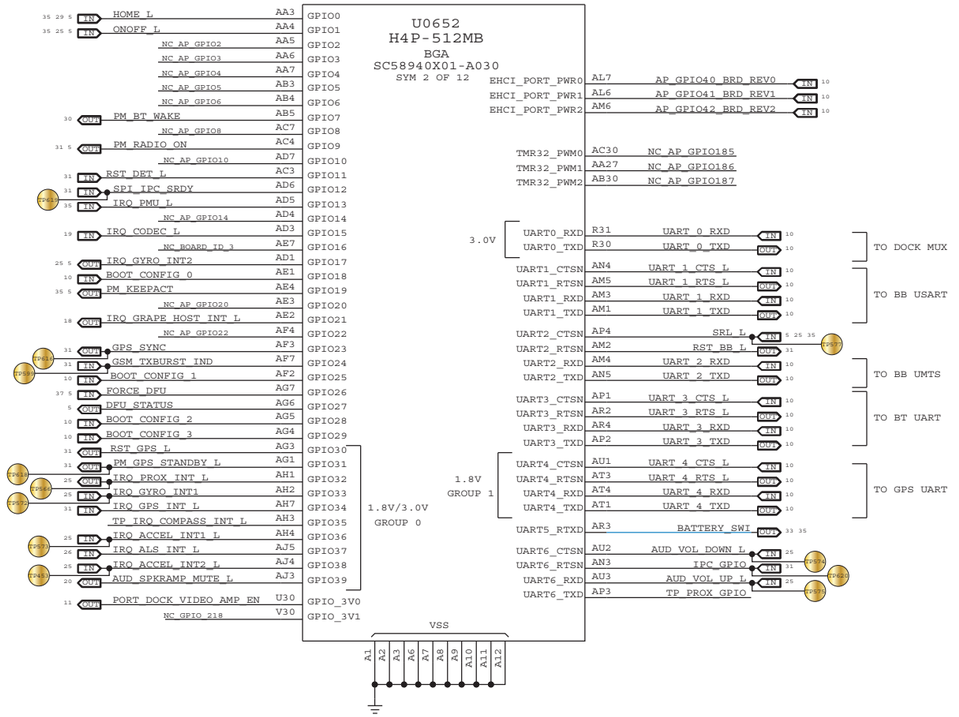
NOTE: PAGE 4608 H4P UM V0.83

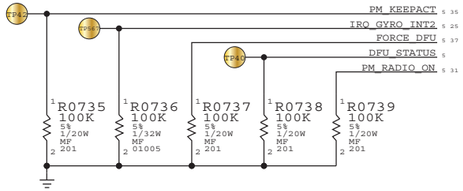
SYNC_MASTER=JAMES	SYNC_DATE=N/A
PAGE TITLE	AP: MAIN
Apple Inc.	DRAWING NUMBER 051-8962 · SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 6 OF 106
	SHEET 4 OF 42

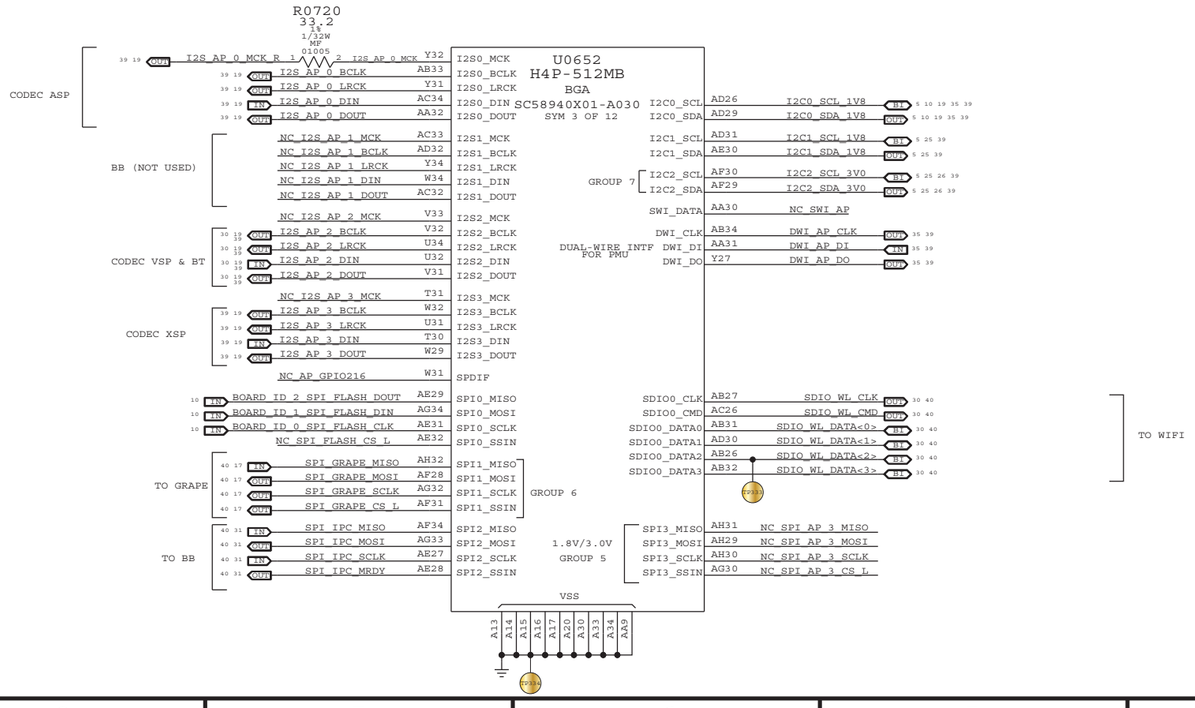
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED











SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE

AP: I/Os

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

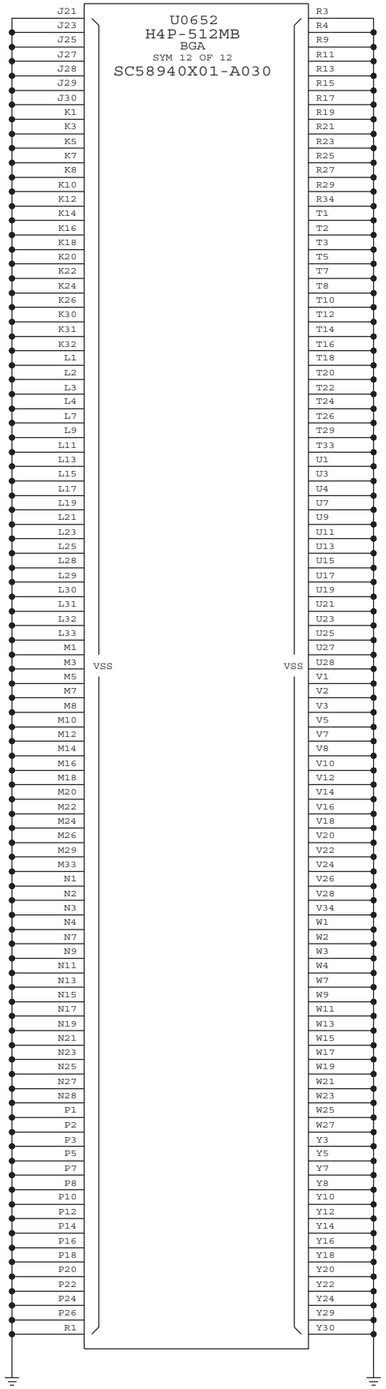
REVISION A.0.0

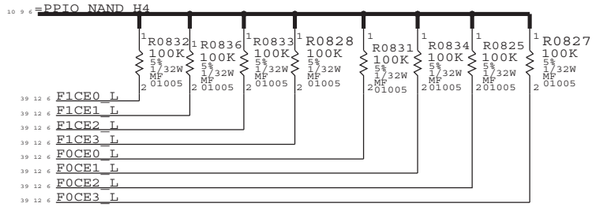
BRANCH

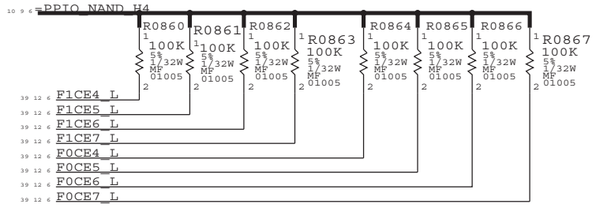
PAGE 7 OF 106

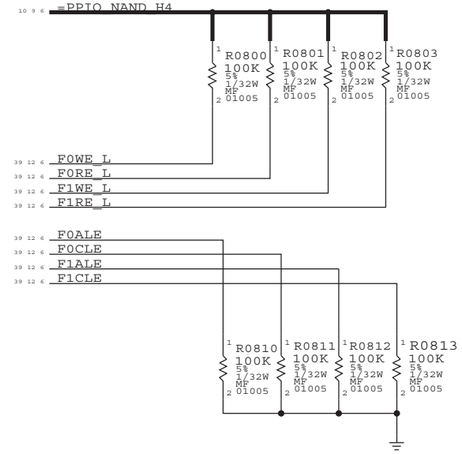
SHEET 5 OF 42

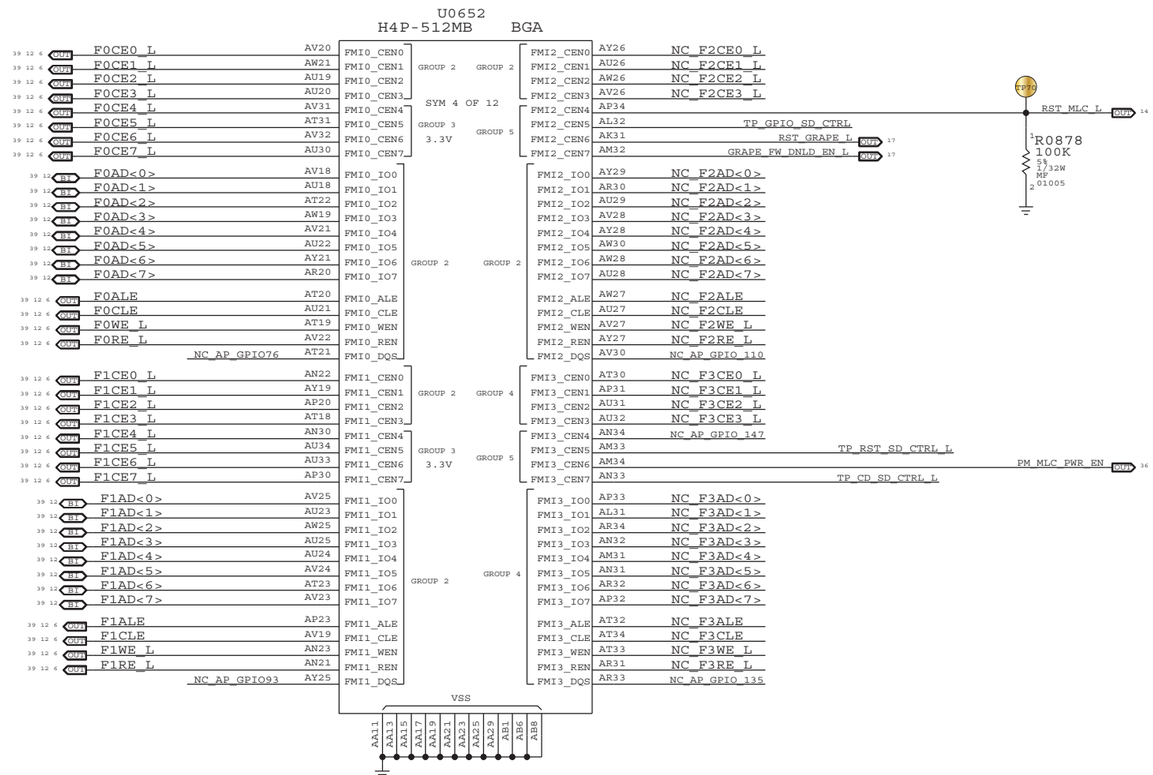
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED











SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE: AP: NAND

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 8 OF 106

SHEET: 6 OF 42

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

MIN_NECK_MIDTH SHOULD BE 0.2MM

=PP3V0_IO_H4
C0954 0.01UF 10% 6.3V X5R 01005
PP_AP_DP_AVDD_AUX
C0927 0.22UF 20% 6.3V X5R 402
C0926 0.22UF 20% 6.3V X5R 402
C0925 0.22UF 20% 6.3V X5R 402
C0924 56PF 5% 6.3V NP0-C0G 01005
R0910 0 5% 1/20W MF 201
=PP1V8_DPORT_H4
C0923 56PF 5% 6.3V NP0-C0G 01005

=PP3V0_VIDEO_H4
C0951 1UF 10% 6.3V CERM 402
C0952 0.01UF 10% 6.3V X5R 01005

PP_DP_PAD_AVDD0
PP_DP_PAD_AVDD1

=PP1V1_DPORT_H4
C0909 0.1UF 10% 6.3V X5R 201

VOLTAGE=1.8V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

FL0910 240-OHM-0.2A-0.8-OHM 0201
=PP3V0_VIDEO_H4
DAC_AP_COMP_PTR
C0955 0.1UF 10% 6.3V X5R 201

DAC_AVDD30A L27 21MA
DAC_AVDD30D K29 6MA
DP_PAD_AVDD_AUX H31 <= 5MA
DP_PAD_AVDD0 E29 63MA
DP_PAD_AVDD1 D30 63MA
DP_PAD_AVDDP0 D31 2MA
DP_PAD_AVDDX G29 5MA
DP_PAD_DVDD J31 1.2MA

SYM 6 OF 12
SC58940X01-A030
U0652
H4P-512MB
BGA

DAC_AP_VREF J33 DAC_VREF
DAC_AP_IREF J34 DAC_IREF
DAC_AP_COMP K34 DAC_COMP
C0956 0.1UF 10% 6.3V X5R 201
R0950 6.34K 1% 1/20W MF 201
TP_DP_AP_ANALOG_TEST H33 DP_PAD_DC_TP
NOTE: 0.6V ANALOG REF
AP_DP_R_BIAS H34 DP_PAD_R_BIAS
C0950 0.01UF 10% 6.3V X5R 01005 NOSTUFF
R0920 4.99K 1% 1/32W MF 01005

DAC_OUT3 L34 DAC_AP_OUT3 OUT 11 YIN
DAC_OUT2 M34 DAC_AP_OUT2 OUT 11 CVBSIN
DAC_OUT1 N34 DAC_AP_OUT1 OUT 11 CIN
DP_HPD R32 DP_AP_HPD IN 13
DP_PAD_AUXP G34 DP_AP_AUX_P BI 13 40
DP_PAD_AUXN F34 DP_AP_AUX_N BI 13 40
DP_PAD_TX0P D34 DP_AP_TX_P<0> OUT 10 13 40
DP_PAD_TX0N C34 DP_AP_TX_N<0> OUT 10 13 40
DP_PAD_TX1P A32 DP_AP_TX_P<1> OUT 10 13 40
DP_PAD_TX1N A31 DP_AP_TX_N<1> OUT 10 13 40

R0955 200 1% 1/20W MF 201
R0956 200 1% 1/20W MF 201
R0957 200 1% 1/20W MF 201
NOTE: PLACE R0955-57 NEAR U0652

DAC_AVSS30A M27
DAC_AVSS30A K27
DAC_AVSS30D K28
DP_PAD_AVSS_AUX G31
DP_PAD_AVSS0 D29
DP_PAD_AVSS1 C30
DP_PAD_AVSSP0 C31
DP_PAD_AVSSX H32
DP_PAD_DVSS J32

=PP1V8_H4
R0930 4.7K 5% 1/32W MF 01005
R0931 4.7K 5% 1/32W MF 01005
R0932 1.00K 5% 1/32W MF 01005
R0933 1.00K 5% 1/32W MF 01005
ISP_AP_0_SCL OUT
ISP_AP_0_SDA BI
ISP_AP_1_SCL OUT
ISP_AP_1_SDA BI

VOLTAGE=0.4V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

=PP1V8_MIPI_H4
C0907 0.1UF 10% 6.3V X5R 201
=PP1V1_MIPI_H4
C0930 1UF 10% 6.3V CERM 402
C0908 0.1UF 10% 6.3V X5R 201
C0903 0.1UF 10% 6.3V X5R 201
MIPI_VDD11 28MA
MIPI0D_VDD18 MIPI1D_VDD18 2MA ???
PP_AP_MIPI0D_0P4V
C0902 2.2NF 10% 10V X5R 201
PP_AP_MIPI1D_0P4V
C0920 2.2NF 10% 10V X5R 201
MIPI0D_VREG_0P4V MIPI1D_VREG_0P4V

NC_AP_GPIO184 AA26 MIPI_VSYNC
MIPI0C_AP_DATA_P<0> IN AW10 MIPI0C_DPDATA0
MIPI0C_AP_DATA_N<0> IN AY10 MIPI0C_DNDATA0
NC_MIPI0C_AP_DATA_P<1> AW11 MIPI0C_DPDATA1
NC_MIPI0C_AP_DATA_N<1> AY11 MIPI0C_DNDATA1
NC_MIPI0C_AP_DATA_P<2> AW13 MIPI0C_DPDATA2
NC_MIPI0C_AP_DATA_N<2> AY13 MIPI0C_DNDATA2
NC_MIPI0C_AP_DATA_P<3> AW14 MIPI0C_DPDATA3
NC_MIPI0C_AP_DATA_N<3> AY14 MIPI0C_DNDATA3
MIPI0C_AP_CLK_P IN AW12 MIPI0C_DPCLK
MIPI0C_AP_CLK_N IN AY12 MIPI0C_DNCLK
REAR CAMERA

MIPID_AP_DATA_P<0> OUT AW5 MIPI0D_DPDATA0
MIPID_AP_DATA_N<0> OUT AY5 MIPI0D_DNDATA0
MIPID_AP_DATA_P<1> OUT AW6 MIPI0D_DPDATA1
MIPID_AP_DATA_N<1> OUT AY6 MIPI0D_DNDATA1
MIPID_AP_DATA_P<2> OUT AW8 MIPI0D_DPDATA2
MIPID_AP_DATA_N<2> OUT AY8 MIPI0D_DNDATA2
MIPID_AP_DATA_P<3> OUT AW9 MIPI0D_DPDATA3
MIPID_AP_DATA_N<3> OUT AY9 MIPI0D_DNDATA3
MIPID_AP_CLK_P OUT AW7 MIPI0D_DPCLK
MIPID_AP_CLK_N OUT AY7 MIPI0D_DNCLK

SYM 5 OF 12
SC58940X01-A030
GROUP 5
U0652
H4P-512MB
BGA

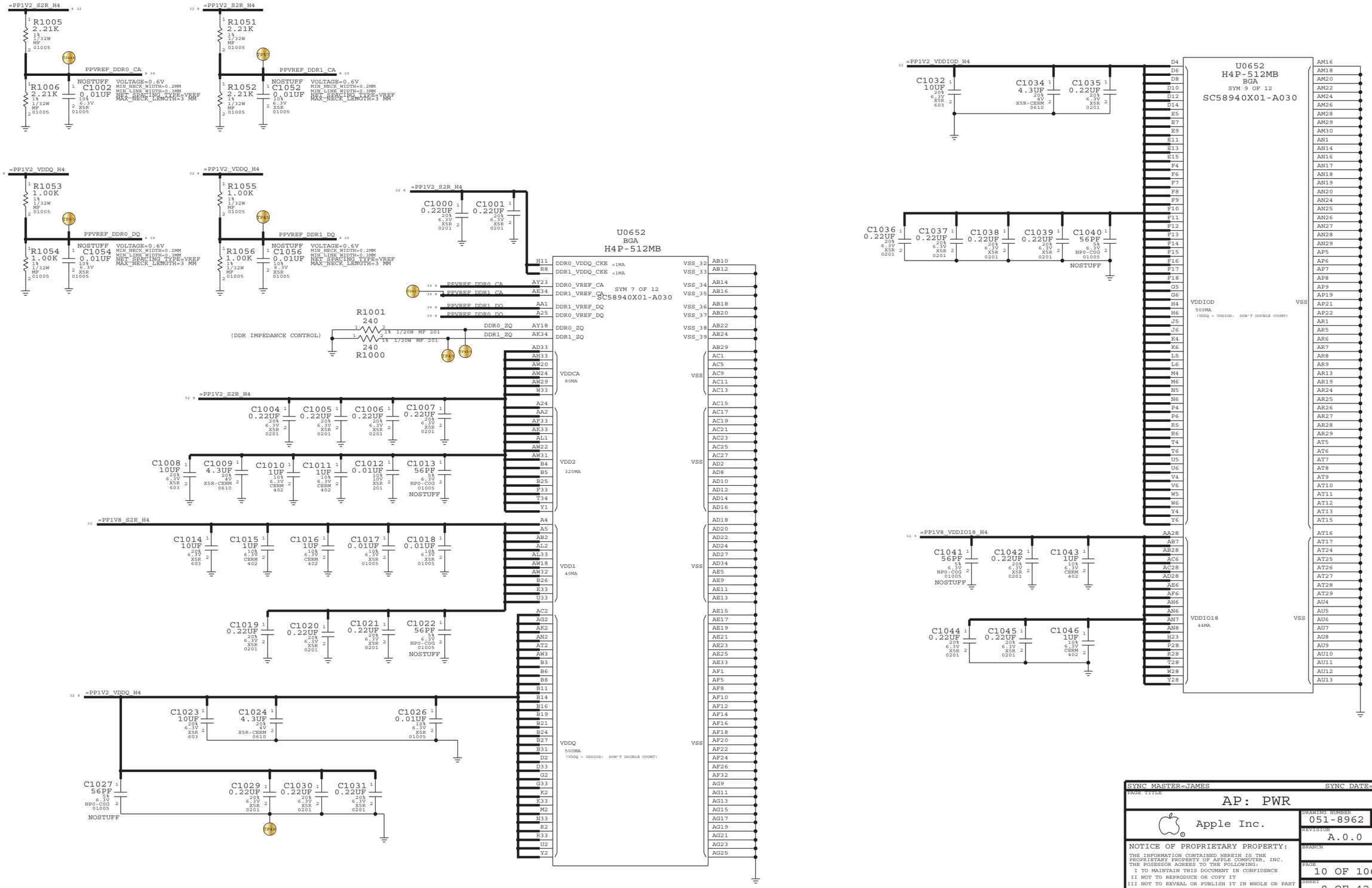
ISP0_FLASH AG31 NC_AP_GPIO153
ISP0_PRE_FLASH AG29 NC_AP_GPIO152
ISP0_SCL AE26 ISP_AP_0_SCL OUT 7 25 39
ISP0_SDA AC29 ISP_AP_0_SDA BI 7 25 39
REAR CAMERA
ISP1_FLASH AJ32 NC_AP_GPIO155
ISP1_PRE_FLASH AG28 NC_AP_GPIO154
ISP1_SCL AC31 ISP_AP_1_SCL OUT 7 26 39
ISP1_SDA AF27 ISP_AP_1_SDA BI 7 26 39
FRONT CAMERA
SENSOR0_CLK AA33 CLK_CAM_RF_R 22 R0900 CLK_CAM_RF OUT 27 39
SENSOR0_RST Y26 PM_REAR_CAM_SHUTDOWN OUT 25
SENSOR1_CLK AA34 CLK_CAM_FF_R 22 R0940 CLK_CAM_FF OUT 26 39
SENSOR1_RST Y33 PM_FRONT_CAM_SHUTDOWN OUT 26

MIPI1C_DPDATA0 AW15 MIPI1C_AP_DATA_P<0> IN 26 40
MIPI1C_DNDATA0 AY15 MIPI1C_AP_DATA_N<0> IN 26 40
MIPI1C_DPDATA1 AW17 NC_MIPI1C_AP_DATA_P<1>
MIPI1C_DNDATA1 AY17 NC_MIPI1C_AP_DATA_N<1>
MIPI1C_DPCLK AW16 MIPI1C_AP_CLK_P OUT 26 40
MIPI1C_DNCLK AY16 MIPI1C_AP_CLK_N OUT 26 40
FRONT CAMERA

MIPI_VSS
AN12 AP12 AR14 AR16 AR17 AR18

SYNC_MASTER=JAMES	SYNC_DATE=N/A
PAGE TITLE: AP: TV,DP,MIPI	
Apple Inc.	DRAWING NUMBER: 051-8962 SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 9 OF 106
	SHEET: 7 OF 42

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE: AP: PWR

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

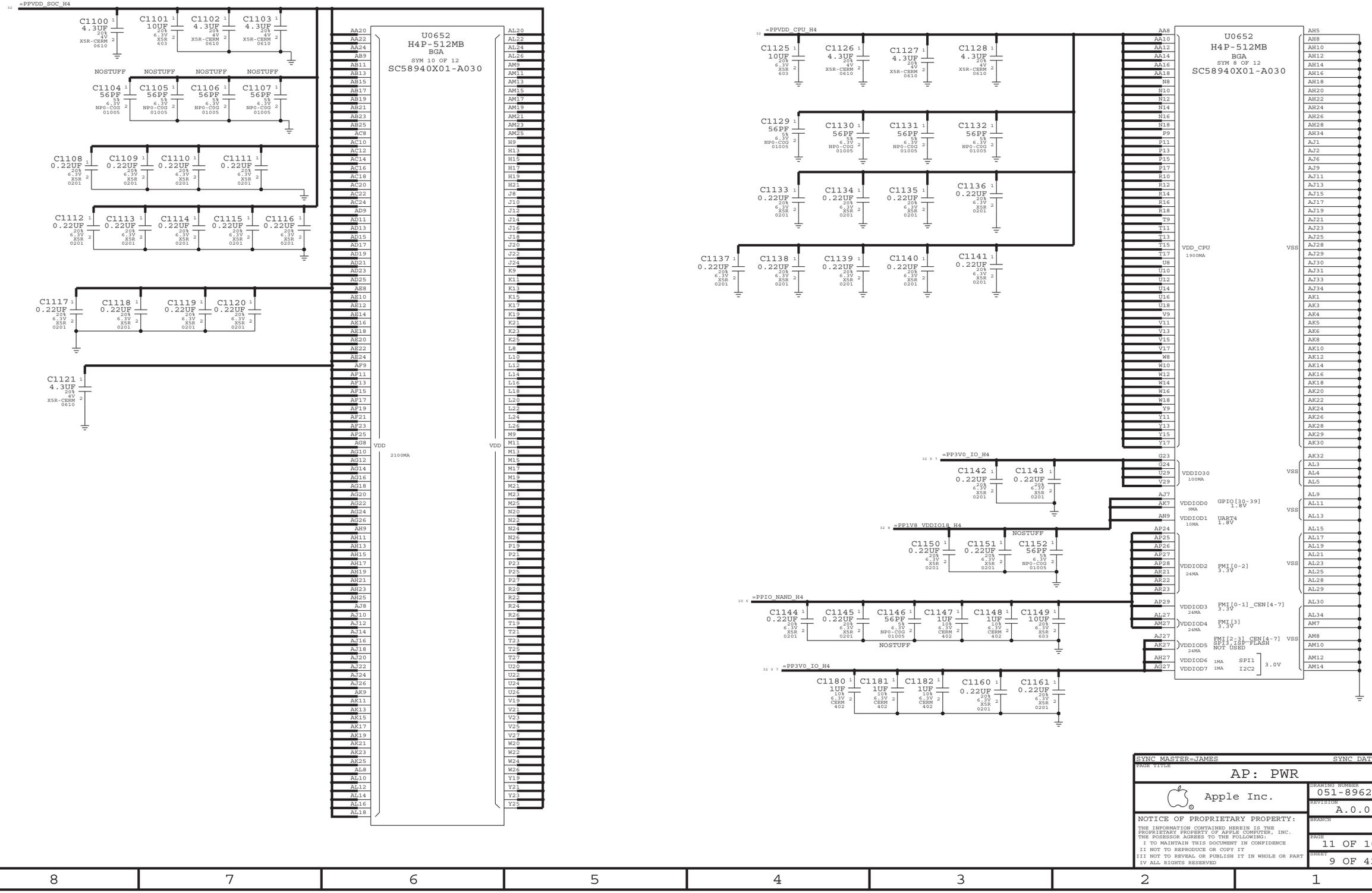
BRANCH:

PAGE: 10 OF 106

SHEET: 8 OF 42

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC MASTER=JAMES SYNC DATE=N/A

PAGE TITLE

AP: PWR

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

BRANCH

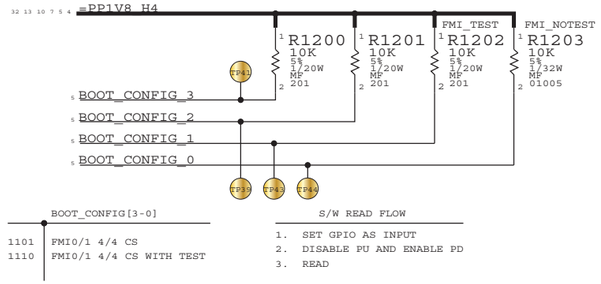
PAGE 11 OF 106

SHEET 9 OF 42

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BOOT CONFIG ID

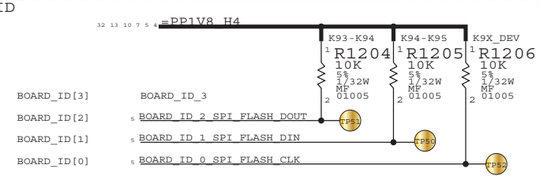


BOOT_CONFIG[3-0]	
1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS WITH TEST

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD ID

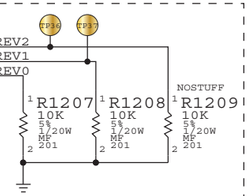


BOARD_ID[3-0]	
0100	K93 AP
0101	K93 DEV
0110	K94 AP
0111	K94 DEV
0010	K95 AP
0011	K95 DEV

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD REVISION



BRD_REV[2-0]	
000	PROTO 1
001	PROTO 2
010	EVT
011	EVT2
100	DVT

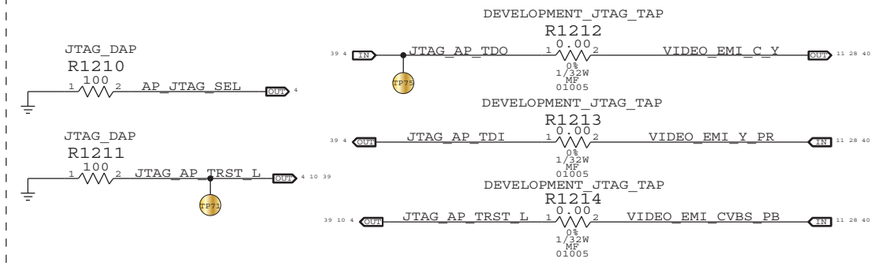
S/W READ FLOW

1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ

FOR REFERENCE

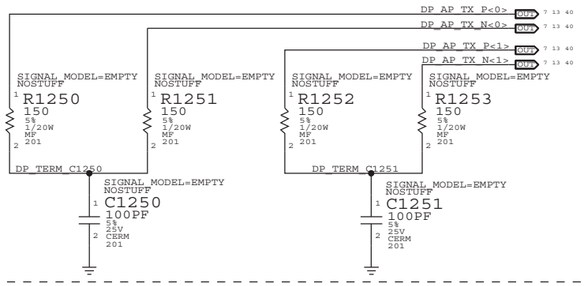
BOOT_CONFIG[3:0]	
0000	SPI0
0001	SPI3
0010	SPI0 W/TEST
0011	SPI3 W/TEST
0100	FMI0 2CS
0101	FMI0 4CS
0110	FMI0 4CS W/TEST
0111	RESERVED
1000	FMI1 2 CS
1001	FMI1 4 CS
1010	FMI1 4CS W/TEST
1011	RESERVED
1100	FMI0/1 2/2 CS
CURRENT SETTING -> 1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS W/TEST
1111	RESERVED

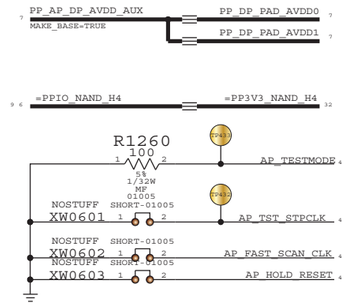
JTAG

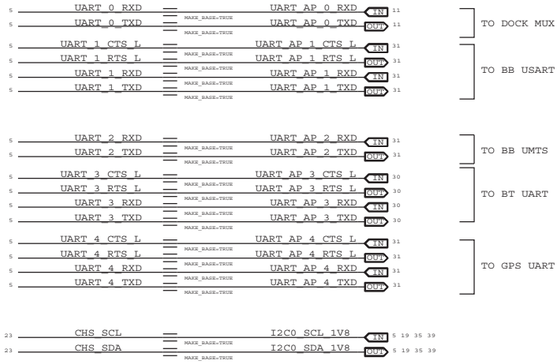


2-WIRE DAP	SCAN DUMP	PRODUCTION
DEVELOPMENT_JTAG JTAG_DAP	DEVELOPMENT_JTAG DEVELOPMENT_JTAG_TAP	JTAG_DAP

PLACEMENT NOTE: NEAR U0652







SYNC_MASTER=JAMES SYNC_DATE=N/A

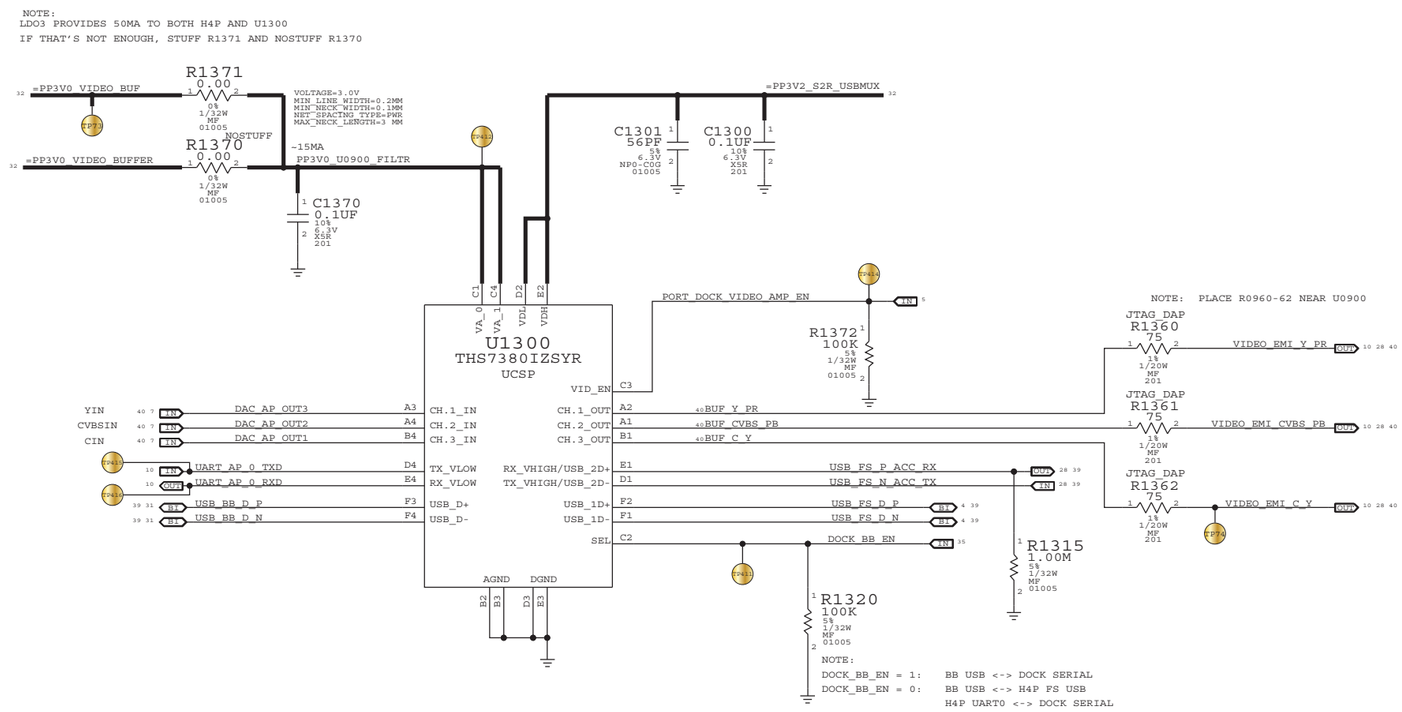
PAGE TITLE
AP: MISC & ALIASES

Apple Inc.

DRAWING NUMBER 051-8962 | SIZE D
REVISION A.0.0
BRANCH
PAGE 12 OF 106
SHEET 10 OF 42

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE
AP: VIDEO BUFFER,BB USB MUXES

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

BRANCH

PAGE 13 OF 106

SHEET 11 OF 42

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	1	TOSHIBA 32NM 16GB RAW	U1400	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	16GB_PROD	U1400	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	16GB_PROD	U1400	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	16GB_PROD	U1400	HYNIX 26NM 16GB PPN

32GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	2	TOSHIBA 32NM 16GB RAW	U1400,U1410	32GB_PROD

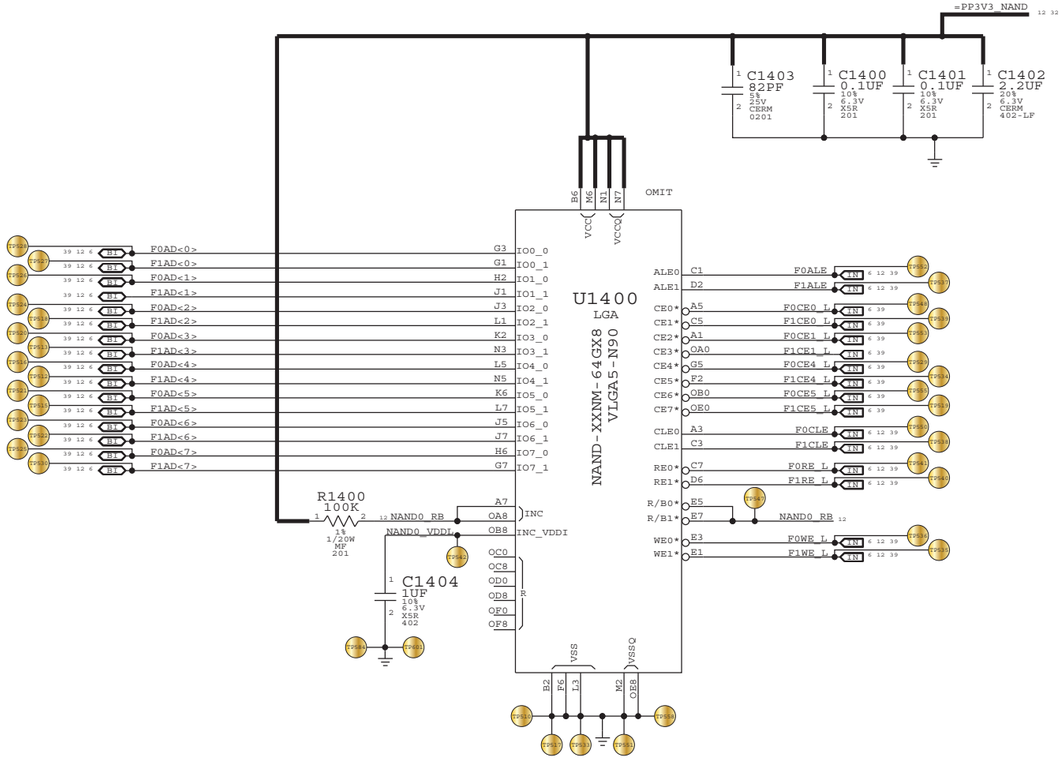
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	32GB_PROD	U1400,U1410	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	32GB_PROD	U1400,U1410	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	32GB_PROD	U1400,U1410	HYNIX 26NM 16GB PPN

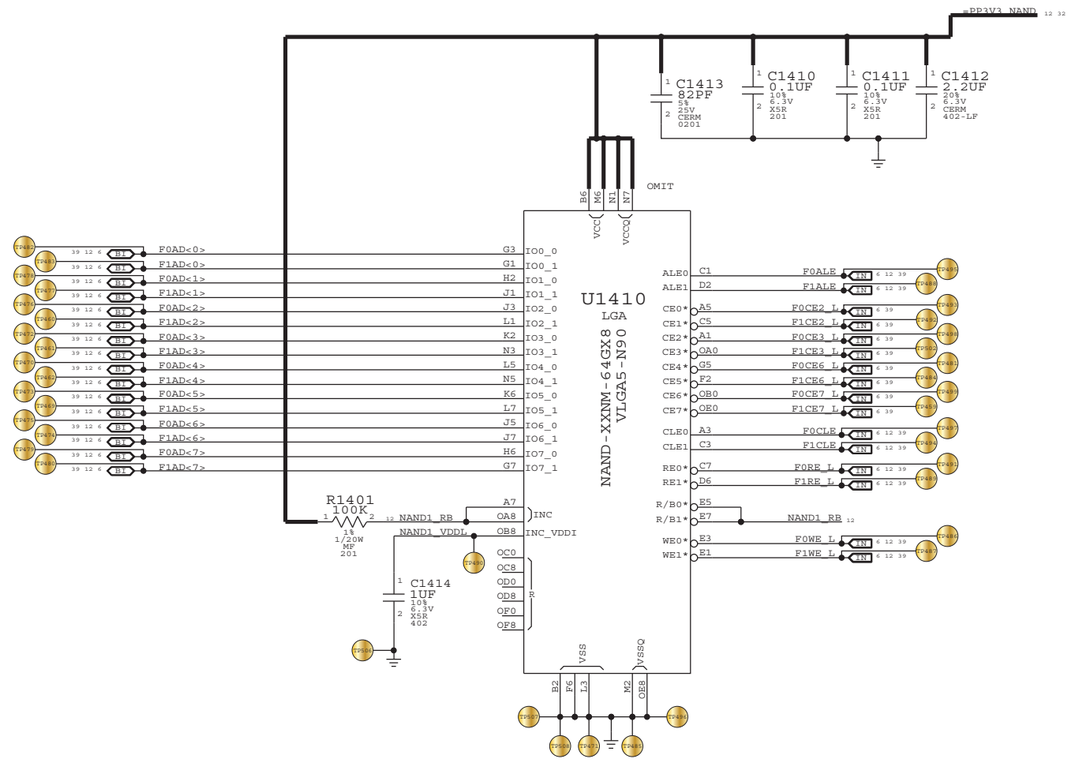
64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0702	2	TOSHIBA 32NM 32GB RAW	U1400,U1410	64GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0665	335S0702	64GB_PROD	U1400,U1410	SAMSUNG 35NM 32GB RAW
335S0791	335S0702	64GB_PROD	U1400,U1410	SAMSUNG 27NM 32GB RAW
335S0722	335S0702	64GB_PROD	U1400,U1410	SANDISK 32NM 32GB RAW
335S0782	335S0702	64GB_PROD	U1400,U1410	HYNIX 26NM 32GB PPN

128GB FLASH CONFIGURATIONS





SYNC MASTER=JONATHAN SYNC DATE=N/A

PAGE TITLE

NAND

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

BRANCH

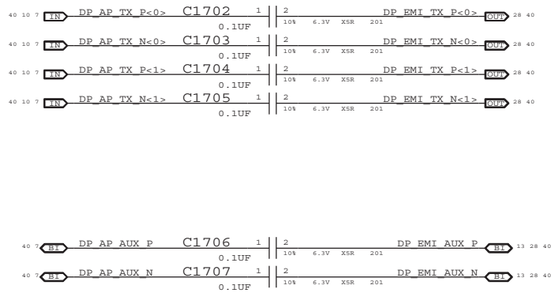
PAGE 14 OF 106

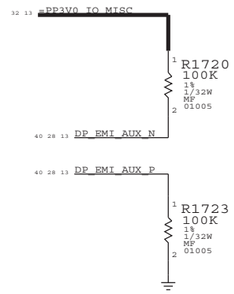
SHEET 12 OF 42

NOTICE OF PROPRIETARY PROPERTY:

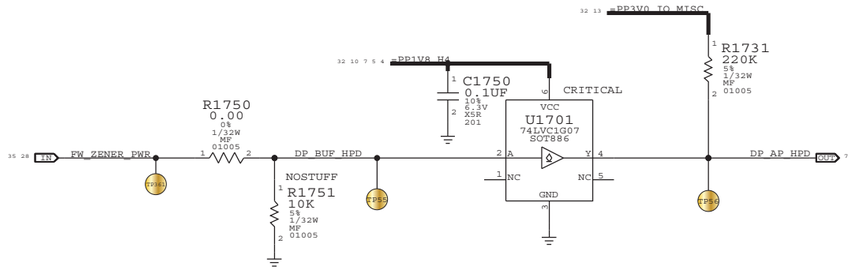
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DISPLAYPORT AC COUPLING





DISPLAYPORT HOT PLUG DETECT



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0536	311S0341		U1701	RADAR:8481319

SYNC MASTER=JAMES SYNC DATE=N/A

PAGE TITLE
VIDEO: DISPLAY PORT

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

BRANCH

PAGE 17 OF 106

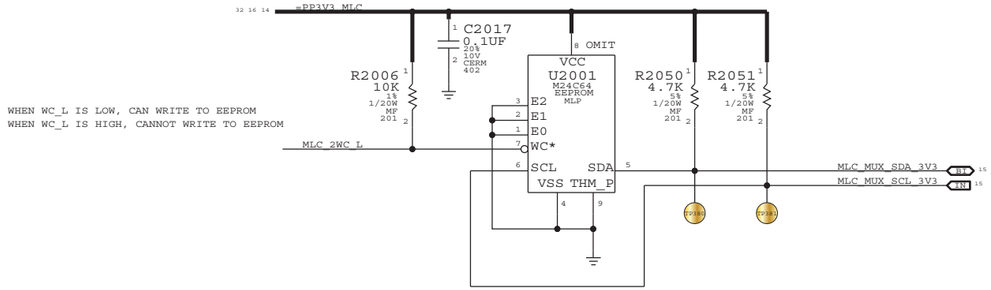
SHEET 13 OF 42

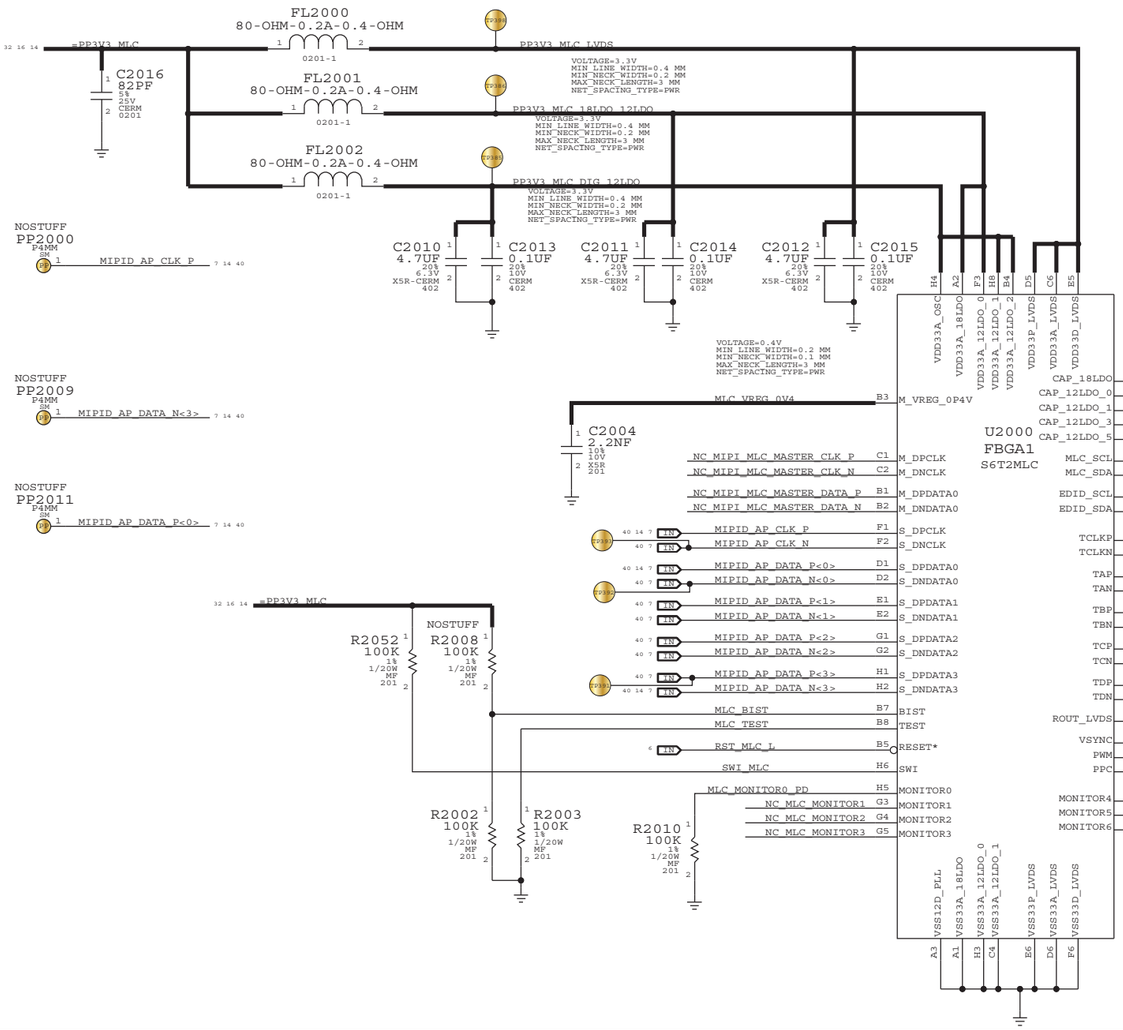
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

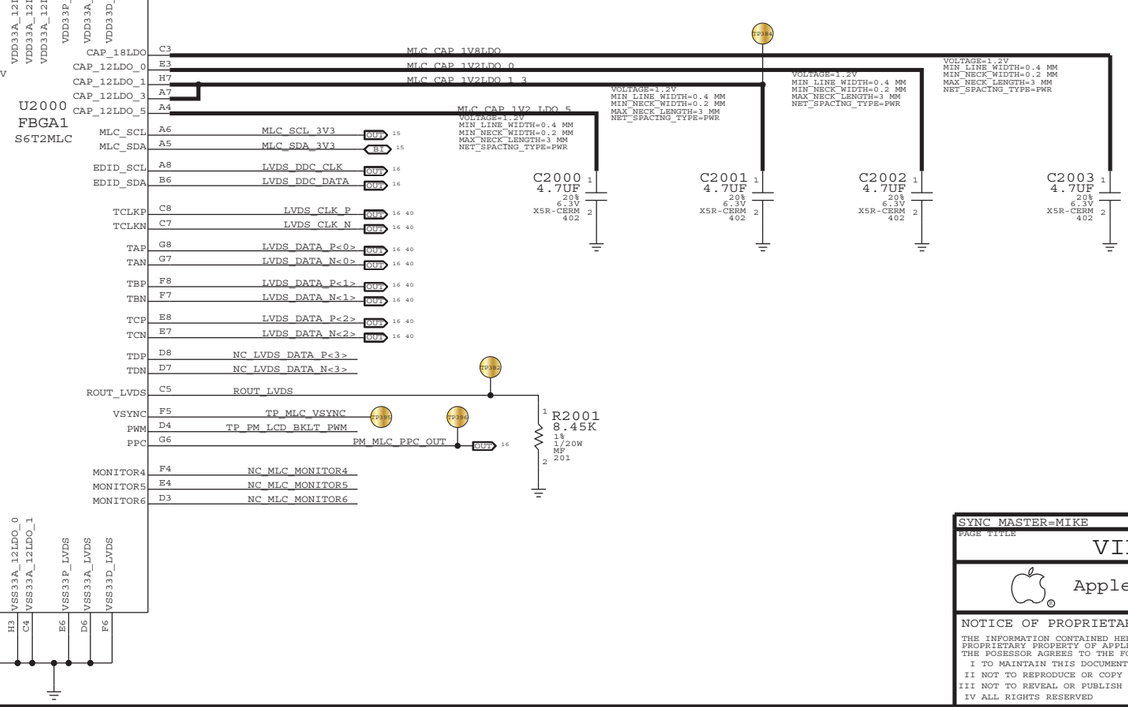
MLC EEPROM:RAW APN 335S0661

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2799	1	MLC EEPROM 100MHZ LVDS,2MHZ SWI	U2001	CRITICAL	100MHZ_PANEL

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0652	138S0618			RADAR:8377307







SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE

VIDEO: MLC

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

BRANCH

PAGE 20 OF 106

SHEET 14 OF 42

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

14 MLC_SDA_3V3 ═══ MLC_MUX_SDA_3V3 14
14 MLC_SCL_3V3 ═══ MLC_MUX_SCL_3V3 14

SYNC_MASTER=MIKE SYNC_DATE=N/A

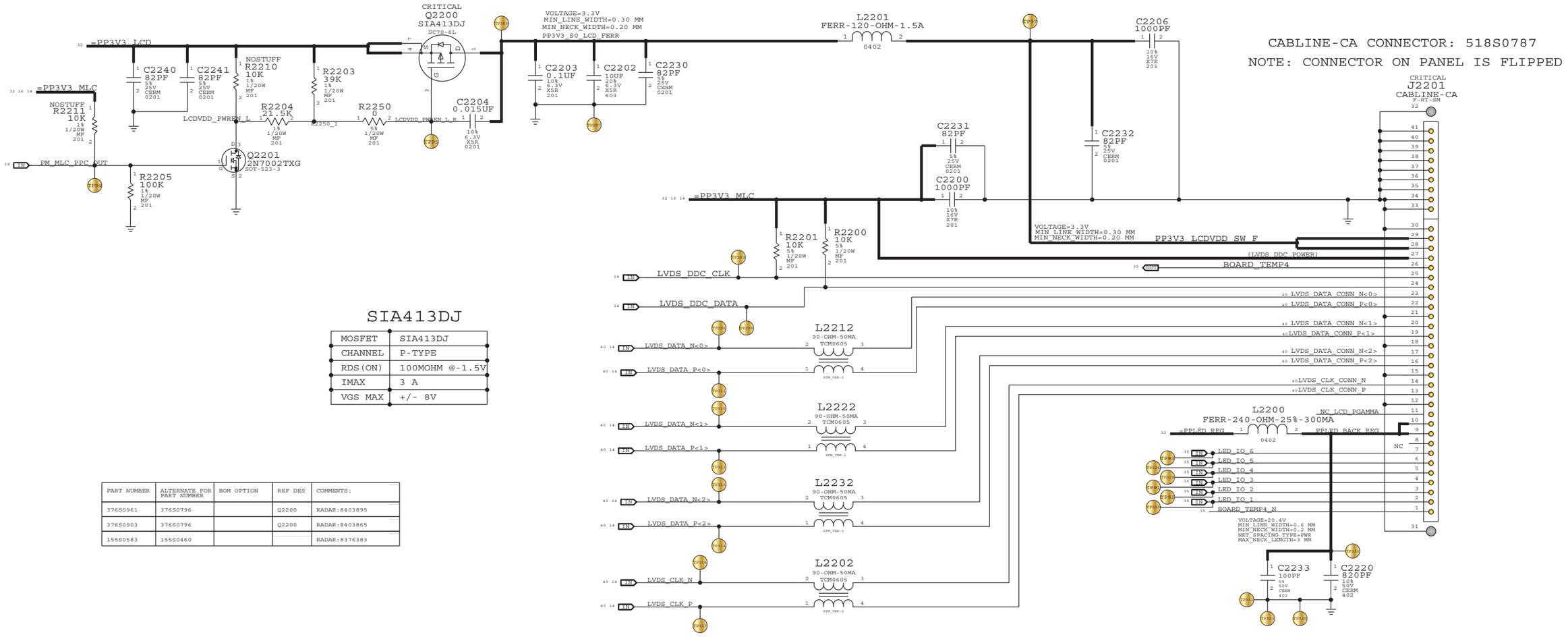
PAGE TITLE
VIDEO: MLC ALIASES

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
PAGE 21 OF 106
SHEET 15 OF 42

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LVDS (LCD) CONNECTOR



CABLINE-CA CONNECTOR: 518S0787

NOTE: CONNECTOR ON PANEL IS FLIPPED

SIA413DJ

MOSFET	SIA413DJ
CHANNEL	P-TYPE
RDS(ON)	100MOHM @-1.5V
IMAX	3 A
VGS MAX	+/- 8V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0961	376S0796		Q2200	RADAR:8403895
376S0903	376S0796		Q2200	RADAR:8403865
155S0583	155S0460			RADAR:8376383

NOSTUFF RESISTORS ARE THERE TO INVESTIGATE POSSIBILITY OF REMOVING THE CHOKE

SYNC_MASTER=ALEX SYNC_DATE=N/A

PAGE TITLE: VIDEO: LVDS CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 22 OF 106

SHEET: 16 OF 42

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0525	1	IC,ASIC,GROUNDHOG B0,120B BGA	U3003	CRITICAL	

(TOUCH SCREEN) CONNECTORS TO GRAPE FLEX

P/N 518S0817

MATES WITH LEFTMOST GRAPE FLEX TAIL

J3010

502250-8237

F-RT-SM

MT_PANEL_OUT<36> 37 — MT_PANEL_OUT<37>
MT_PANEL_OUT<38> 35 — MT_PANEL_OUT<39>
MT_PANEL_IN<29> 33 — 32
MT_PANEL_IN<27> 31 — MT_PANEL_IN<28>
MT_PANEL_IN<25> 29 — MT_PANEL_IN<26>
MT_PANEL_IN<23> 27 — MT_PANEL_IN<24>
MT_PANEL_IN<21> 25 — MT_PANEL_IN<22>
MT_PANEL_IN<19> 23 — MT_PANEL_IN<20>
MT_PANEL_IN<17> 21 — MT_PANEL_IN<18>
MT_PANEL_IN<15> 19 — MT_PANEL_IN<16>
MT_PANEL_IN<13> 17 — MT_PANEL_IN<14>
MT_PANEL_IN<11> 15 — MT_PANEL_IN<12>
MT_PANEL_IN<9> 13 — MT_PANEL_IN<10>
MT_PANEL_IN<7> 11 — MT_PANEL_IN<8>
MT_PANEL_IN<5> 9 — MT_PANEL_IN<6>
MT_PANEL_IN<3> 7 — MT_PANEL_IN<4>
MT_PANEL_IN<1> 5 — MT_PANEL_IN<2>
3 — MT_PANEL_IN<0>
1
41
39
38
40

MATES WITH RIGHTMOST GRAPE FLEX TAIL

J3011

502250-8237

F-RT-SM

MT_PANEL_OUT<1> 37 — MT_PANEL_OUT<0>
MT_PANEL_OUT<3> 35 — MT_PANEL_OUT<2>
MT_PANEL_OUT<5> 33 — MT_PANEL_OUT<4>
MT_PANEL_OUT<7> 31 — MT_PANEL_OUT<6>
MT_PANEL_OUT<9> 29 — MT_PANEL_OUT<8>
MT_PANEL_OUT<11> 27 — MT_PANEL_OUT<10>
MT_PANEL_OUT<13> 25 — MT_PANEL_OUT<12>
MT_PANEL_OUT<15> 23 — MT_PANEL_OUT<14>
MT_PANEL_OUT<17> 21 — MT_PANEL_OUT<16>
MT_PANEL_OUT<19> 19 — MT_PANEL_OUT<18>
MT_PANEL_OUT<21> 17 — MT_PANEL_OUT<20>
MT_PANEL_OUT<23> 15 — MT_PANEL_OUT<22>
MT_PANEL_OUT<25> 13 — MT_PANEL_OUT<24>
MT_PANEL_OUT<27> 11 — MT_PANEL_OUT<26>
MT_PANEL_OUT<29> 9 — MT_PANEL_OUT<28>
MT_PANEL_OUT<31> 7 — MT_PANEL_OUT<30>
MT_PANEL_OUT<33> 5 — MT_PANEL_OUT<32>
MT_PANEL_OUT<35> 3 — MT_PANEL_OUT<34>
1
41
39
38
40

PP18V_GRAPE
C3005 0.1UF 10% 25V X5R 402
C3007 0.1UF 10% 25V X5R 402
C3053 0.1UF 10% 25V X5R 402
F3 E3 B6 A6
VDDH
VCC_DIG
=PP3V0_GRAPE_MARIO
C3006 0.1UF 10% 6.3V X5R 201

U3003
GROUNDHOG
BGA
CRITICAL
I DON'T WANT TO OMIT!
Texas Instruments
CD3240B0

MUX_IN<0> B1 MUX0
MUX_IN<1> C1 MUX1
MUX_IN<2> E1 MUX2
MUX_IN<3> F2 MUX3
MUX_IN<4> H1 MUX4
MUX_IN<5> J1 MUX5
MUX_IN<6> J2 MUX6
MUX_IN<7> J3 MUX7
MUX_IN<8> K4 MUX8
MUX_IN<9> H5 MUX9
MUX_IN<10> I5 MUX10
MUX_IN<11> J8 MUX11
MUX_IN<12> J9 MUX12
MUX_IN<13> K8 MUX13
MUX_IN<14> J10 MUX14
MUX_IN<15> I10 MUX15
MUX_IN<16> H10 MUX16
MUX_IN<17> F11 MUX17
MUX_IN<18> C11 MUX18
MUX_IN<19> E10 MUX19
NC A11 MUX20
NC B4 MUX21
NC A5 MUX22
NC A2 MUX23

Z1_BON_L<0> C7 BON_L0
Z1_BON_L<1> A7 BON_L1
Z1_BON_L<2> B7 BON_L2
Z1_BON_L<3> B8 BON_L3
Z1_BON_L<4> A8 BON_L4
Z1_BON_L<5> C8 BON_L5

NC C6
NC D3
NC D4
NC D5
NC D6
NC D8
NC D9
NC E4
NC E8
NC F4
NC F5
NC F8
NC F9
NC G3
NC G4
NC G9
NC H3
NC H4
NC H7
NC H8
NC H9
NC J6
NC K7
NC

VSTM0 A1 MT_PANEL_OUT<0>
VSTM1 B2 MT_PANEL_OUT<1>
VSTM2 C2 MT_PANEL_OUT<2>
VSTM3 D1 MT_PANEL_OUT<3>
VSTM4 D2 MT_PANEL_OUT<4>
VSTM5 E2 MT_PANEL_OUT<5>
VSTM6 F1 MT_PANEL_OUT<6>
VSTM7 G1 MT_PANEL_OUT<7>
VSTM8 G2 MT_PANEL_OUT<8>
VSTM9 I1 MT_PANEL_OUT<9>
VSTM10 H2 MT_PANEL_OUT<10>
VSTM11 I2 MT_PANEL_OUT<11>
VSTM12 K1 MT_PANEL_OUT<12>
VSTM13 K2 MT_PANEL_OUT<13>
VSTM14 I3 MT_PANEL_OUT<14>
VSTM15 K3 MT_PANEL_OUT<15>
VSTM16 J4 MT_PANEL_OUT<16>
VSTM17 I4 MT_PANEL_OUT<17>
VSTM18 K6 MT_PANEL_OUT<18>
VSTM19 H6 MT_PANEL_OUT<19>
VSTM20 K5 MT_PANEL_OUT<20>
VSTM21 J5 MT_PANEL_OUT<21>
VSTM22 I7 MT_PANEL_OUT<22>
VSTM23 K9 MT_PANEL_OUT<23>
VSTM24 I8 MT_PANEL_OUT<24>
VSTM25 K10 MT_PANEL_OUT<25>
VSTM26 I6 MT_PANEL_OUT<26>
VSTM27 J7 MT_PANEL_OUT<27>
VSTM28 K11 MT_PANEL_OUT<28>
VSTM29 I9 MT_PANEL_OUT<29>
VSTM30 J11 MT_PANEL_OUT<30>
VSTM31 I11 MT_PANEL_OUT<31>
VSTM32 H11 MT_PANEL_OUT<32>
VSTM33 G11 MT_PANEL_OUT<33>
VSTM34 G10 MT_PANEL_OUT<34>
VSTM35 F10 MT_PANEL_OUT<35>
VSTM36 C10 MT_PANEL_OUT<36>
VSTM37 D10 MT_PANEL_OUT<37>
VSTM38 E11 MT_PANEL_OUT<38>
VSTM39 D11 MT_PANEL_OUT<39>
VSTM40 B11 NC
VSTM41 B10 NC
VSTM42 C4 NC
VSTM43 A4 NC
VSTM44 B5 NC
VSTM46 A3 NC
VSTM45 C5 NC
VSTM47 B3 NC

A_AD_R0 A10 Z1_B_ADR<0>
A_AD_R1 B9 Z1_B_ADR<1>
A_AD_R2 A9 Z1_B_ADR<2>

GND
G8 G7 G6 G5 F7 F6 E7 E6 E5 B3 D7 C9

BOOST CONVERTOR

MIN NECK MIDTH SHOULD BE 0.4MM

L3000 4.7UH-700MA-280MOHM
MIN_LINE_WIDTH=0.2MM
VR_BOOST_L — VR_BOOST_SW
VLF

D3000 SOD-323 B0520WSXG

PP18V_R_GRAPE
HET_SPACING_TYPE=PWR
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=18V

LOAD CURRENT ~ 153UA
R3066 0.1 1% 1/20W MF 201
PP18V_GRAPE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=18V
HET_SPACING_TYPE=PWR

=PP3V0_GRAPE
C3009 0.1UF 10% 16V X5R 402
C3008 33PF 5% 25V NP0-C0G 201
R3009 1M 1% 1/16W MF-LF 402
C3000 1UF 10% 25V X5R 603-1
R3012 71.5K 1% 1/20W MF 201
C3002 470PF 10% 16V X5R-X7R 201
C3001 2.2UF 10% 6.3V X5R 603

CRITICAL
U3000 TPS61045 QFN-1
VIN
NC DO L FB VR_BOOST_FBK
CTRL PM_BOOST_EN
SW
THRML PAD PGND GND
AGND_U3000
MIN_LINE_WIDTH=0.2MM
XW3000 SM

=PP3V0_GRAPE
R3025 10K 5% 1/20W MF 201
SPI_GRAPE_SCLK — GRAPE_SCLK
SPI_GRAPE_CS_L — GRAPE_CS_L
SPI_GRAPE_MOSI — GRAPE_MOSI
RST_GRAPE_L — RST_GRAPE_Z1_L
RST_GRAPE_Z2_L
TO Z2
SPI_GRAPE_MISO — GRAPE_MISO
MAKE_BASE=TRUE

=PP3V0_GRAPE
R3030 10K 5% 1/20W MF 201
R3031 10K 5% 1/20W MF 201
C3030 0.1UF 10% 6.3V X5R 201
C3031 0.1UF 10% 6.3V X5R 201
R3032 3.3K 5% 1/20W MF 201
R3033 10K 5% 1/20W MF 201
CRITICAL
VCCA VCCB
U3007 PQFP1
SN74AVCH4T245RSV
DIR_U3007
1A1 SPI_GRAPE_SCLK
2A1 SPI_GRAPE_CS_L
1DIR
1OE*
1A2 SPI_GRAPE_MOSI
2A2
2DIR
2OE*
GRAPE_FW_DNLD_EN_L
(A -> B)
GND
1B1 Z1_SCLK
2B1 Z2_H_CS_L
1B2 Z1_MISO
2B2 Z1_CS_OE
TO Z1/Z2
APN:311S0485

=PP3V0_GRAPE
C3050 0.1UF 10% 6.3V X5R 201
CRITICAL
VCC
U3010 SN74LVC1G126DRYR-M LLP
Z1_CS_OE — OE
Z2_H_CS_L — A
Y — Z1_CS_L
GND NC

=PP3V0_GRAPE
C3041 0.1UF 10% 6.3V X5R 201
CRITICAL
U3009 SN74LVC1G125DRYR-M LLP
SPI_GRAPE_MISO — OE*
NC
Z1_MOSI
Z1_CS_OE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0523	311S0485		U3007	
311S0524	311S0533		U3009	
311S0525	311S0532		U3010	

SYNC_MASTER=RAMSIN SYNC_DATE=N/A

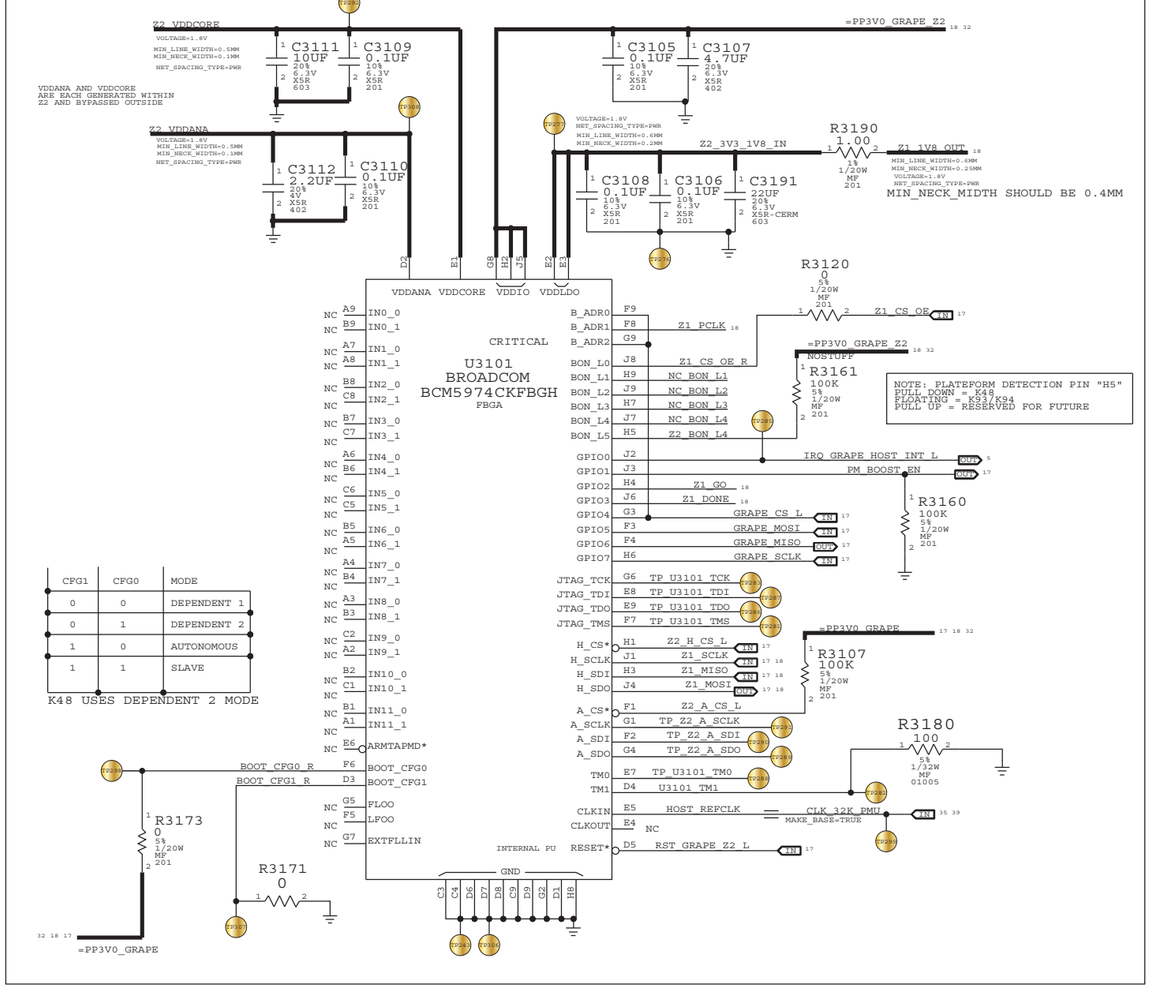
PAGE TITLE
GRAPE: GROUNDHOG,CONN,BOOST

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
PAGE 30 OF 106
SHEET 17 OF 42

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

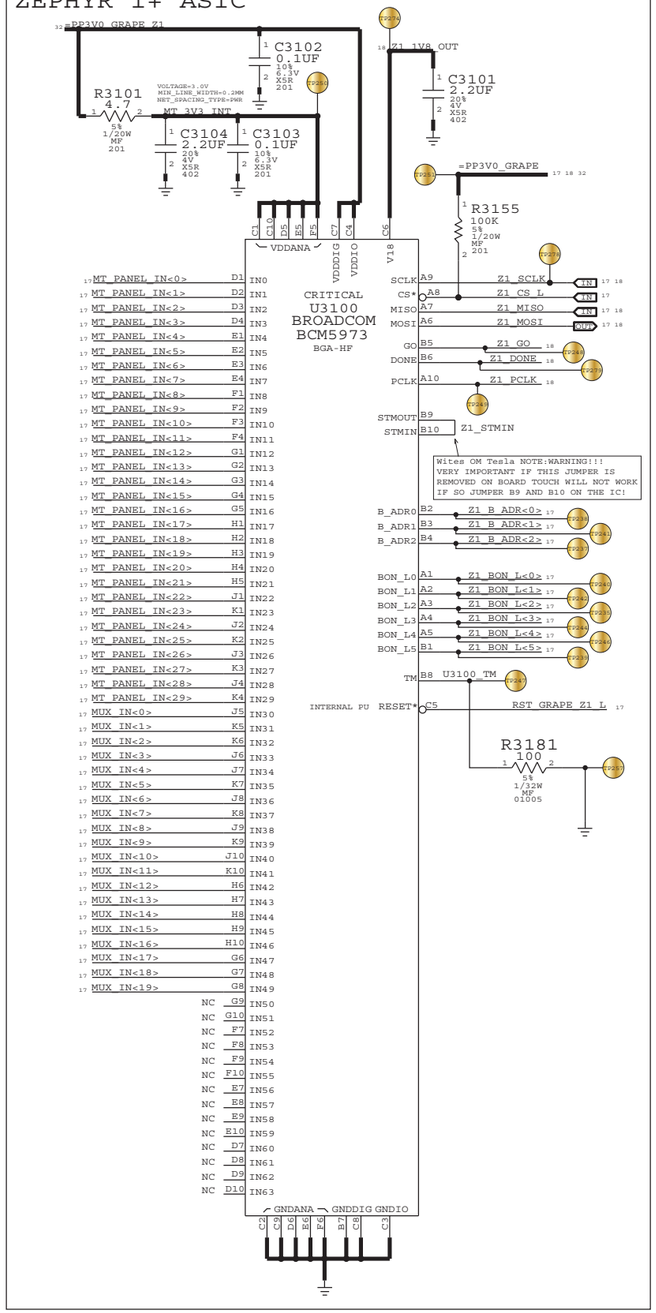
ARM9 MCU (Z2 BASED)



CFG1	CFG0	MODE
0	0	DEPENDENT 1
0	1	DEPENDENT 2
1	0	AUTONOMOUS
1	1	SLAVE

K48 USES DEPENDENT 2 MODE

ZEPHYR 1+ ASIC



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0652	138S0648		C3107	RADAR:8392120
138S0618	138S0648		C3107	BOM CONSOLIDATION

SYNC_MASTER=RAMSIN SYNC_DATE=N/A

PAGE TITLE: GRAPE: Z1, Z2

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 31 OF 106

SHEET: 18 OF 42

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

L63 AUDIO CODEC

APN:338S0940

=PPVCC_MAIN_AUDIO
=PP1V8_AUDIO
=PP1V7_VA_VCP

C3600 1000PF 10% 6.3V X5R 01005
C3601 0.1UF 20% 4V X5R 01005
C3602 0.1UF 20% 4V X5R 01005
C3603 10UF 20% 6.3V X5R 603
C3604 0.1UF 10% 6.3V X5R 201
C3605 27PF 5% 16V NPO-COG 01005
C3606 10UF 20% 4V X5R 402
C3607 0.1UF 20% 4V X5R 01005
C3608 4.7UF 20% 4V TANT 402-3

XW3600 SM
XW3601 SM
XW3602 SM
GND_AUDIO_CODEC

MIN_LINE_WIDTH=1.0MM
MIN_NECK_WIDTH=0.2MM
GND_AUDIO_HP_AMP

U3600
CS42L63B
WLCSP

I2C ADDRESS: 1001010X??

VD B11
VL C11
VP F5
VA G2
VCP D11

I2C0_SCL_1V8 IN → SCL C6
I2C0_SDA_1V8 BI → SDA C7
IRQ_CODEC_L OUT ← INT* E4
RST_L63_L IN → RESET* E5
AUD_MIK_HS1_INT_L OUT ← WAKE* E3
I2S_AP_0_MCK_R IN → MCLK B9
I2S_AP_0_LRCK IN → ASP_LRCLK C8
I2S_AP_0_BCLK IN → ASP_SCLK B7
I2S_AP_0_DOUT IN → ASP_SDIN B8
I2S_AP_0_DIN OUT ← ASP_SDOUT A9
I2S_AP_2_LRCK IN → VSP_LRCLK C9
I2S_AP_2_BCLK IN → VSP_SLCLK C10
I2S_AP_2_DOUT IN → VSP_SDIN A11
I2S_AP_2_DIN OUT ← VSP_SDOUT A10
I2S_AP_3_LRCK IN → XSP_LRCLK B6
I2S_AP_3_BCLK IN → XSP_SCLK A6
I2S_AP_3_DOUT IN → XSP_SDIN/DAC2B_MUTE A8
I2S_AP_3_DIN OUT ← XSP_SDOUT A7

R3601 22 5% 1/32W MF 01005 — L63_ASP_SDOUT
R3602 22 5% 1/32W MF 01005 — L63_VSP_SDOUT
R3603 22 5% 1/32W MF 01005 — L63_XSP_SDOUT

DMIC_SCLK_SENSOR OUT ← R3608 NOSTUFF 22 5% 1/32W MF 01005 → DMIC_SCLK_CODEC B5
DMIC_SCLK_CANADA OUT ← R3620 22 5% 1/32W MF 01005
DMIC_SD_SENSOR IN → R3621 NOSTUFF 22 5% 1/32W MF 01005 → DMIC_SD_CODEC A5
DMIC_SD_CANADA IN → R3622 22 5% 1/32W MF 01005
DMIC_SD DMIC_SD
NC_LINE_IN1_CODEC LINEINA C5
NC_LINE_IN1_REF_CODEC LINEINA_REF C4
NC_LINE_IN2_CODEC LINEINB D6
NC_LINE_IN2_REF_CODEC LINEINB_REF D5
NC_MIC1_BIAS_CODEC MIC1_BIAS D4
NC_MIC1P_CODEC MIC1 A3
NC_MIC1N_CODEC MIC1_REF B3
NC_MIC1_FILT_CODEC MIC1_BIAS_FILT E2

EXT_MIC_BIAS OUT ← MIC2_BIAS C2
HSMIC_C_P IN → MIC2_DETECT D3
EXT_MIC_P IN → MIC2 B1
EXT_MIC_REF IN → MIC2_REF B2
HSMIC_C_N IN → MIC2_DETECT_REF C3

R3604 1.00K 1% 1/32W MF 01005 — MIC2_DET
R3605 1.00K 1% 1/32W MF 01005 — MIC2_DET_REF

MIC2_BIAS_FILT C1
MIC3A_BIAS D2
MIC3A A1
MIC3A_REF A2
MIC3A_BIAS_FILT D1
MIC3B_BIAS F1
MIC3B A4
MIC3B_REF B4
MIC3B_BIAS_FILT E1

C3611 4.7UF 20% 6.3V X5R-CERM 402
C3609 4.7UF 20% 6.3V X5R-CERM 402

GNDD B10
GNDA F2
GNDCP E10
GNDP G5
GND D8
GND D9

HP_DETECT E9 → HP_DET IN
HPOUTB G9 → HP_R OUT
HPOUTA G10 → HP_L OUT
HPOUT_REF F9 → HP_REF IN
LINEOUT1B G8 → CODEC_LINE_OUT_R OUT
LINEOUT1A F8 → CODEC_LINE_OUT_L OUT
LINEOUT1_REF E8 → CODEC_LINE_OUT_REF IN
LINEOUT2A D7 → LEFT_CH_OUT_P OUT
LINEOUT2A_REF E7 → LEFT_CH_OUT_REF IN
LINEOUT2B F7 → RIGHT_CH_OUT_P OUT
LINEOUT2B_REF G7 → RIGHT_CH_OUT_REF IN

EAROUT+ G3 → NC_EAROUT_AP
EAROUT- F3 → NC_EAROUT_AN
SPEAKEROUTA+ F6 → NC_SPEAKEROUT_AP
SPEAKEROUTA- G6 → NC_SPEAKEROUT_AN
SPEAKEROUTB+ F4 → NC_SPEAKEROUT_BP
SPEAKEROUTB- G4 → NC_SPEAKEROUT_BN

FLYP E11 VHP_FLYP
FLYC F11 VHP_FLYC
FLYN G11 VHP_FLYN

C3617 2.2UF 20% 10V X5R-CERM 402
C3618 2.2UF 20% 10V X5R-CERM 402

SPEAKER_VQ E6 SPKR_VQ — NOT USING SPEAKER AMPLIFIER, THIS CAN BE A NO STUFF
FILT+ G1 FILT_P

+VCP_FILT D10 VHPPFILT
-VCP_FILT F10 VHPNFILT

C3614 10UF 20% 6.3V X5R 603
C3613 10UF 20% 6.3V X5R 603
CRITICAL C3615 1UF 10% 6.3V TANT 402-1
2.2UF RECOMMENDED CRITICAL C3616 4.7UF 20% 6.3V X5R-CERM 402

GND_AUDIO_CODEC
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
MAX_NECK_LENGTH=75 MM

SYNC MASTER=LENG	SYNC DATE=N/A
PAGE TITLE: AUDIO: L63 CODEC	
Apple Inc.	DRAWING NUMBER 051-8962 SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 36 OF 106
	SHEET 19 OF 42

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

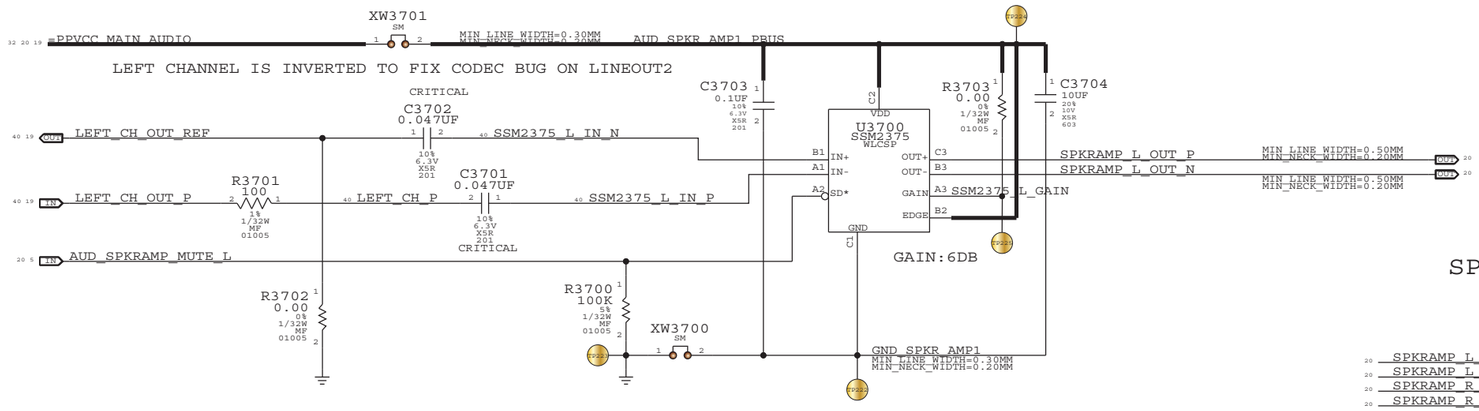
GAIN	VDD	GND
12DB	47K	NC
9DB	NC	47K
6DB	SHORT	NC
3DB	NC	NC
0DB	NC	SHORT

SPEAKER AMPLIFIER 1

APN:353S2958

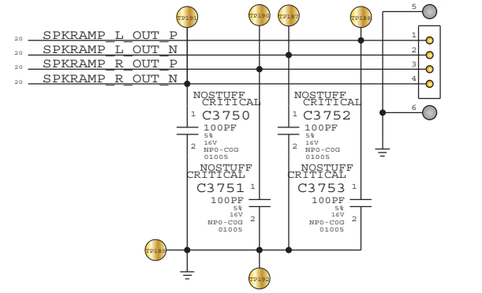
TURN ON TIME: 7.5MS

80HZ +/- XXX% TURN ON DELAY: 20MS



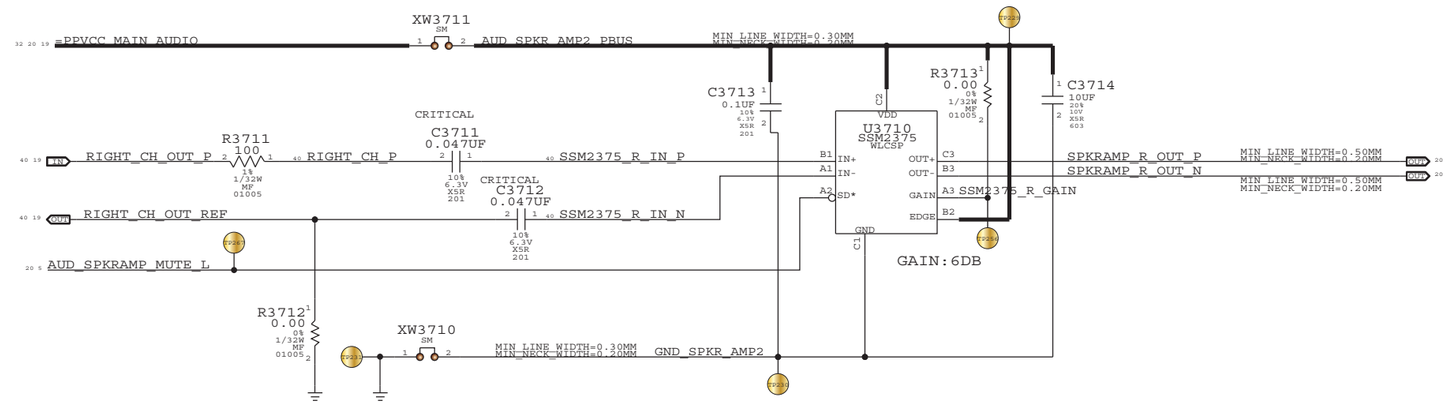
SPEAKER CONNECTOR

APN 518S0521



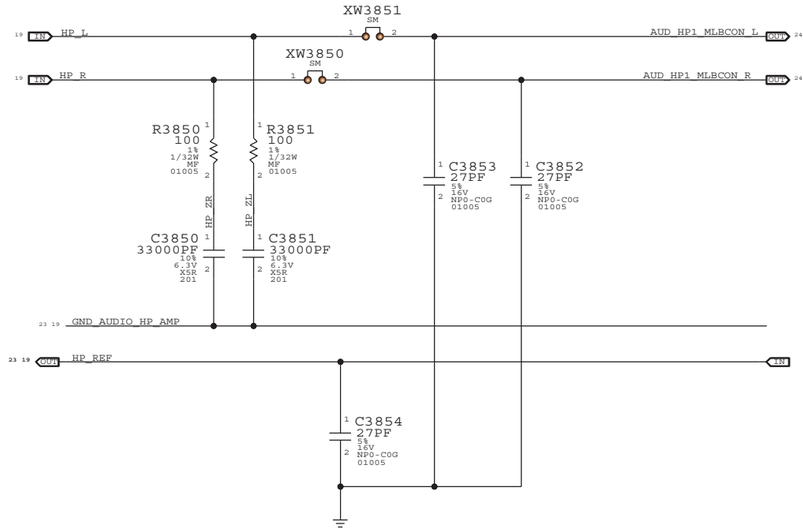
L63 LINEOUT2A IS CONNECTED TO U3700
L63 LINEOUT2B IS CONNECTED TO U3710

SPEAKER AMPLIFIER 2

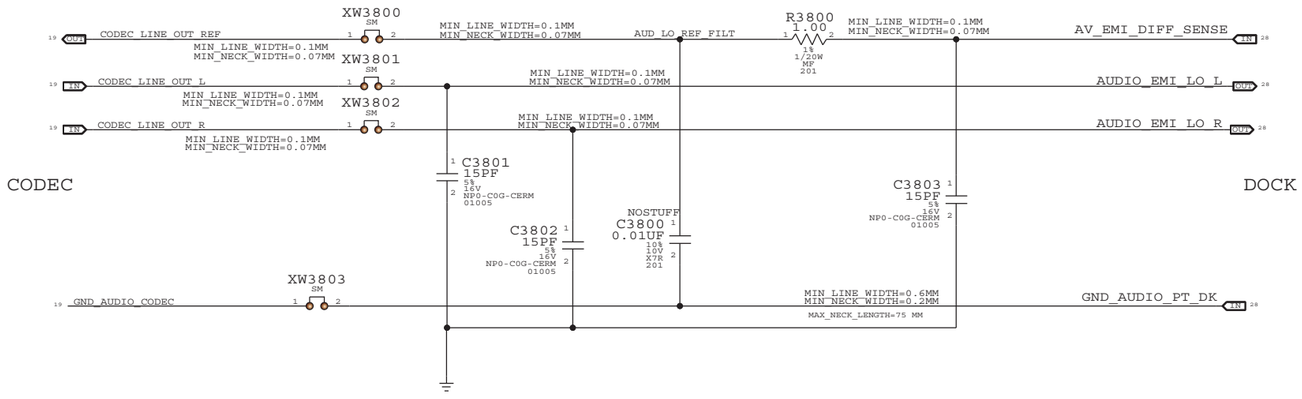


SYNC MASTER=LENG	SYNC DATE=N/A
PAGE TITLE: AUDIO: SPEAKER AMP	
Apple Inc.	DRAWING NUMBER: 051-8962 SIZE: D
	REVISION: A.0.0
NOTICE OF PROPRIETARY PROPERTY:	BRANCH:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	PAGE: 37 OF 106
	SHEET: 20 OF 42

HEADPHONE OUTPUT ZOBEL NETWORK



DOCK LINE OUTPUT



SYNC_MASTER=LENG SYNC_DATE=N/A

PAGE TITLE
AUDIO: HEADPHONE OUT

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
PAGE 38 OF 106
SHEET 21 OF 42

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SYNC_MASTER=LENG SYNC_DATE=N/A

PAGE TITLE

AUDIO: BLANK

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

BRANCH

PAGE 39 OF 106

SHEET 22 OF 42

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:

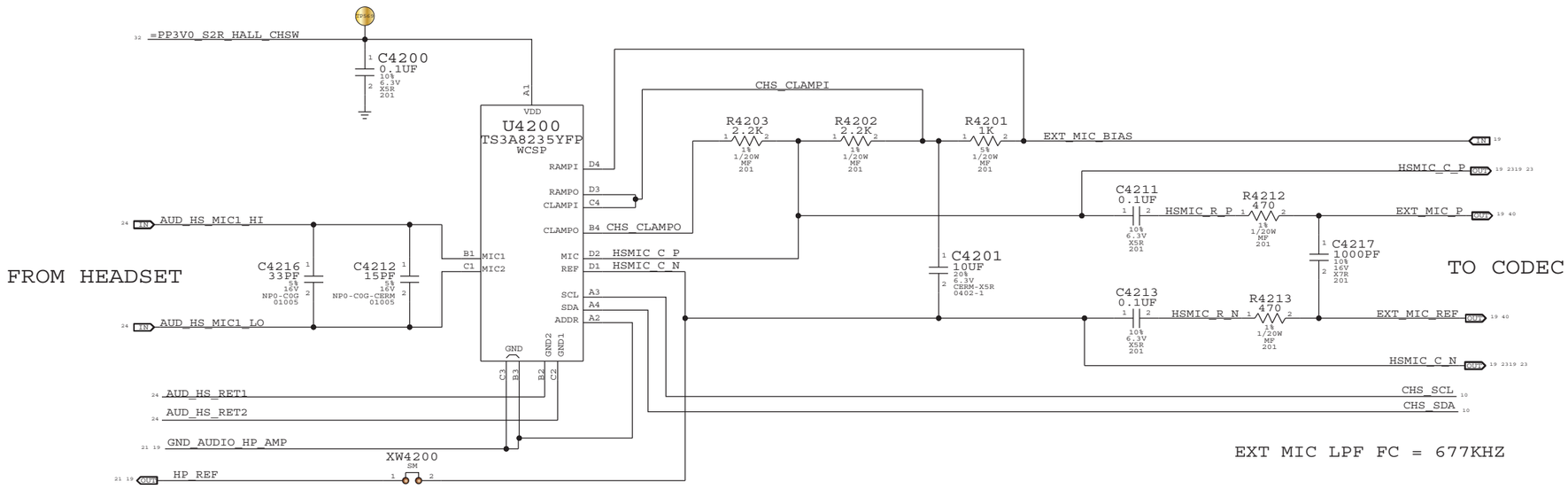
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

IV ALL RIGHTS RESERVED

EXTERNAL (HEADSET) MIC INPUT CIRCUITRY



EXT MIC LPF FC = 677KHZ

SYNC_MASTER=LENG SYNC_DATE=N/A

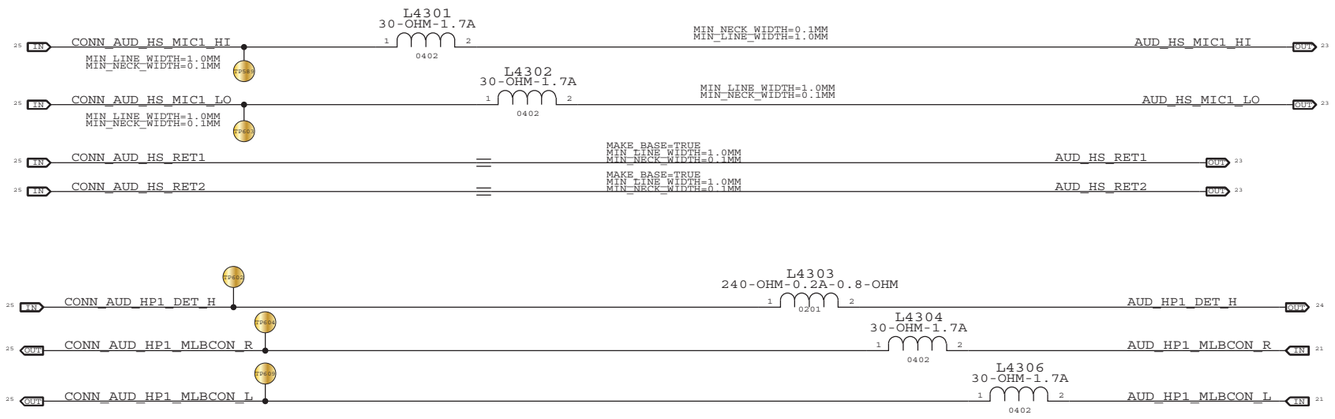
PAGE TITLE
AUDIO: DETECT/MIC BIAS

Apple Inc.

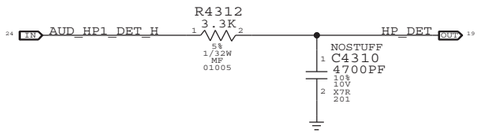
DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
PAGE 42 OF 106
SHEET 23 OF 42

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

HEADPHONE JACK CONNECTION IS ON FRONT PANEL FLEX, CSA 55/PDF 29
PLACE ALL COMPONENTS NEAR J5501



HEADSET JACK INSERTION DETECT



SYNC MASTER=LENG
SYNC DATE=N/A

PAGE TITLE
AUDIO: HP/MIC FILTERS

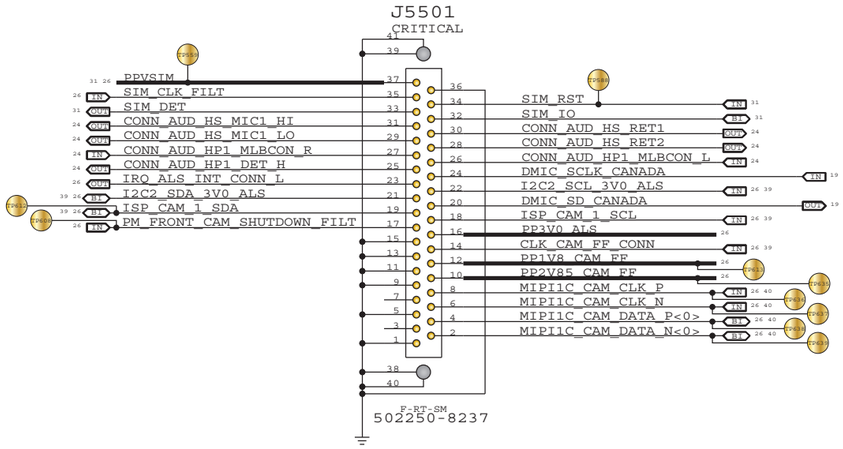
Apple Inc.

DRAWING NUMBER 051-8962
SIZE D
REVISION A.0.0
BRANCH
PAGE 43 OF 106
SHEET 24 OF 42

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

CANADA FLEXES CONN.

APN: 518S0817



SENSOR BOARD CONN ALIASES

39 27	CLK_CAM_RF_FILT	MAKE_BASE=TRUE	CONN_CLK_CAM_RF_FILT	27
40 27	MIPI0C_CAM_DATA_N<0>	MAKE_BASE=TRUE	CONN_MIPI0C_CAM_DATA_N<0>	27
40 27	MIPI0C_CAM_DATA_P<0>	MAKE_BASE=TRUE	CONN_MIPI0C_CAM_DATA_P<0>	27
		MAKE_BASE=TRUE		
40 27	MIPI0C_CAM_CLK_N	MAKE_BASE=TRUE	CONN_MIPI0C_CAM_CLK_N	27
40 27	MIPI0C_CAM_CLK_P	MAKE_BASE=TRUE	CONN_MIPI0C_CAM_CLK_P	27
7	PM_REAR_CAM_SHUTDOWN	MAKE_BASE=TRUE	CONN_PM_REAR_CAM_SHUTDOWN	27
27	PP1V8_SENSOR_FILT	MAKE_BASE=TRUE	CONN_PP1V8_SENSOR_FILT	27
27	PP2V85_CAM_REAR	MAKE_BASE=TRUE	CONN_PP2V85_CAM_REAR	27
19	DMIC_SD_SENSOR	MAKE_BASE=TRUE	CONN_DMIC_SD_SENSOR	27
19	DMIC_SCLK_SENSOR	MAKE_BASE=TRUE	CONN_DMIC_SCLK_SENSOR	27
39 7	ISP_AP_0_SCL	MAKE_BASE=TRUE	CONN_ISP_AP_0_SCL	27
39 7	ISP_AP_0_SDA	MAKE_BASE=TRUE	CONN_ISP_AP_0_SDA	27
39 26 5	I2C2_SCL_3V0	MAKE_BASE=TRUE	CONN_I2C2_SCL_3V0	27
39 26 5	I2C2_SDA_3V0	MAKE_BASE=TRUE	CONN_I2C2_SDA_3V0	27
5	IRQ_ACCEL_INT1_L	MAKE_BASE=TRUE	CONN_IRQ_ACCEL_INT1_L	27
5	IRQ_ACCEL_INT2_L	MAKE_BASE=TRUE	CONN_IRQ_ACCEL_INT2_L	27
5	IRQ_GYRO_INT1	MAKE_BASE=TRUE	CONN_IRQ_GYRO_INT1	27
5	IRQ_GYRO_INT2	MAKE_BASE=TRUE	CONN_IRQ_GYRO_INT2	27
39 5	I2C1_SCL_1V8	MAKE_BASE=TRUE	CONN_I2C1_SCL_1V8	27
39 5	I2C1_SDA_1V8	MAKE_BASE=TRUE	CONN_I2C1_SDA_1V8	27
35	IRQ_HALL	MAKE_BASE=TRUE	CONN_IRQ_HALL	27
5	IRQ_PROX_INT_L	MAKE_BASE=TRUE	CONN_IRQ_PROX_INT_L	27
27	PP3V0_S2R_HALL_FILT	MAKE_BASE=TRUE	CONN_PP3V0_S2R_HALL	27
35 5	ONOFF_L	MAKE_BASE=TRUE	CONN_ONOFF_FTR_L	27
35 5	SRL_L	MAKE_BASE=TRUE	CONN_SRL_FTR_L	27
5	AUD_VOL_UP_L	MAKE_BASE=TRUE	CONN_AUD_VOL_UP_FTR_L	27
5	AUD_VOL_DOWN_L	MAKE_BASE=TRUE	CONN_AUD_VOL_DOWN_FTR_L	27
		MAKE_BASE=TRUE		
27	PP3V0_OPTICAL_SENS	MAKE_BASE=TRUE	CONN_PP3V0_OPTICAL_SENS	27

SYNC_MASTER=MARK B. SYNC_DATE=N/A

PAGE TITLE

CONNECTOR: CANADA FLEX CONN,SENSOR PANEL ALIASES

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

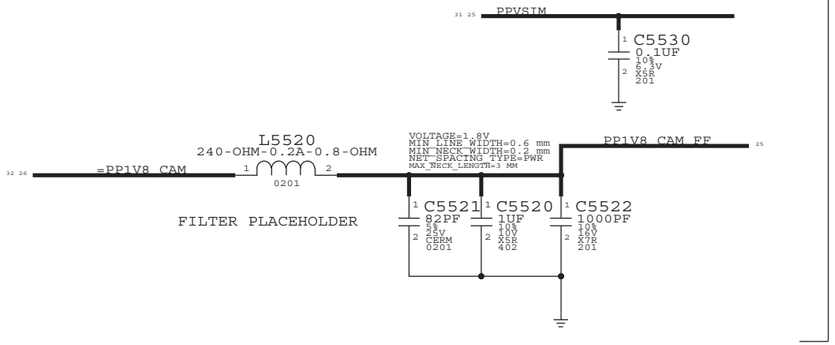
BRANCH

PAGE 54 OF 106

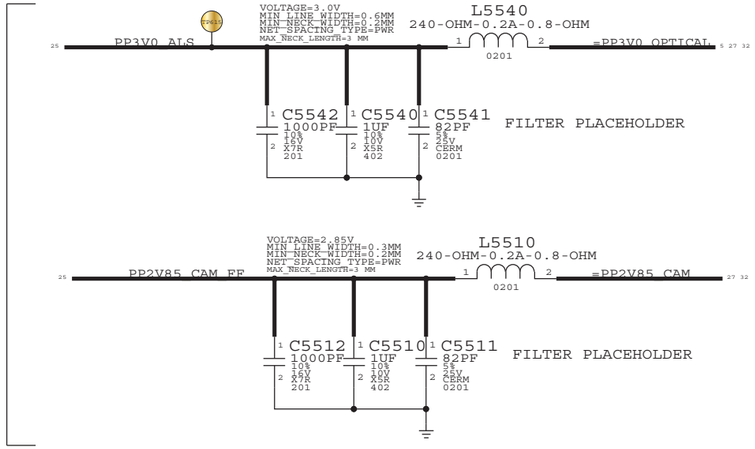
SHEET 25 OF 42

NOTICE OF PROPRIETARY PROPERTY:

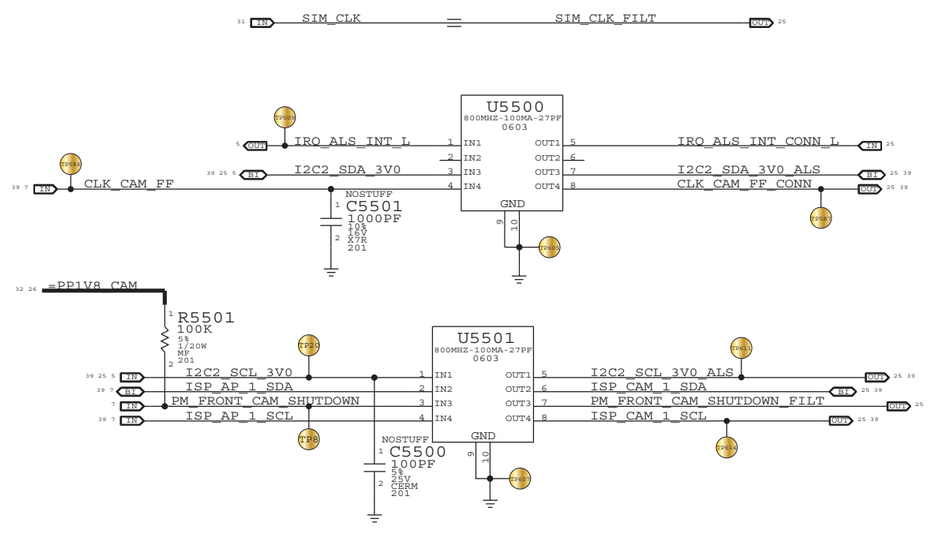
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

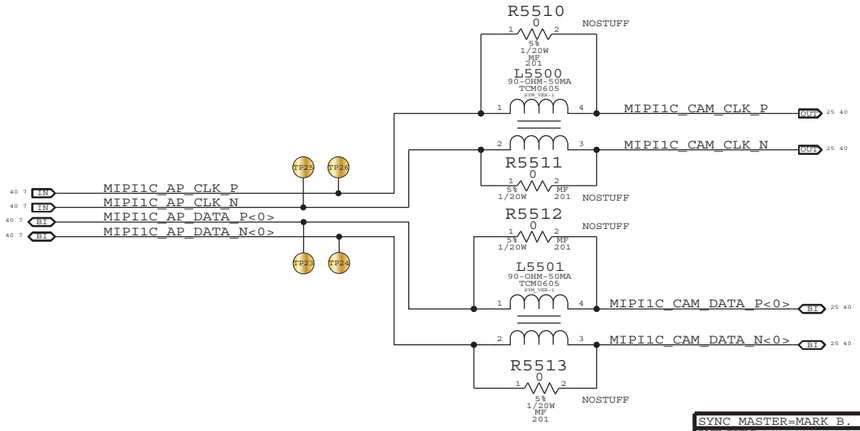


CANADA FLEX CONN ON PG 54



CANADA FLEX SIGNAL FILTERS





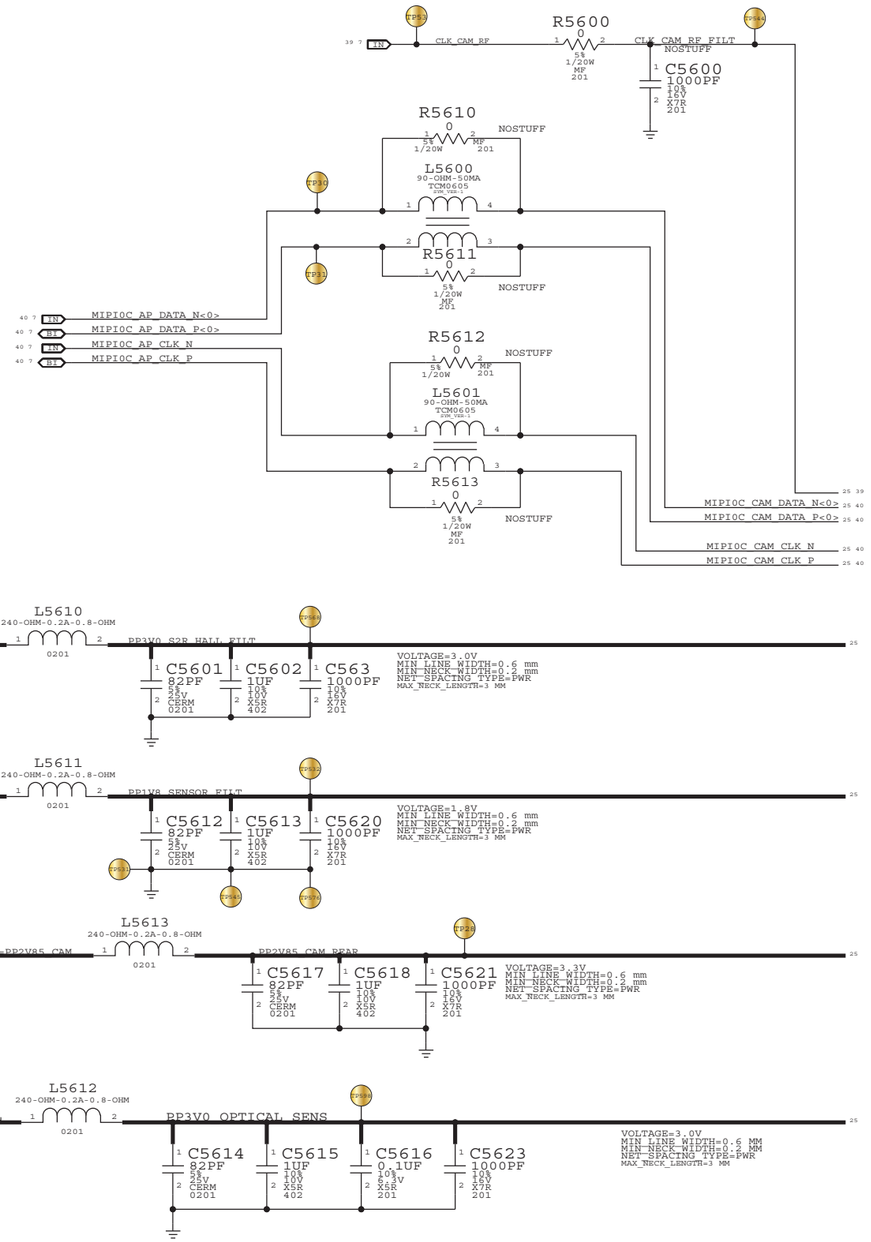
SYNC_MASTER=MARK_B. SYNC_DATE=N/A

PAGE TITLE
CONNECTOR: CANADA FLEX FILTERS

Apple Inc.

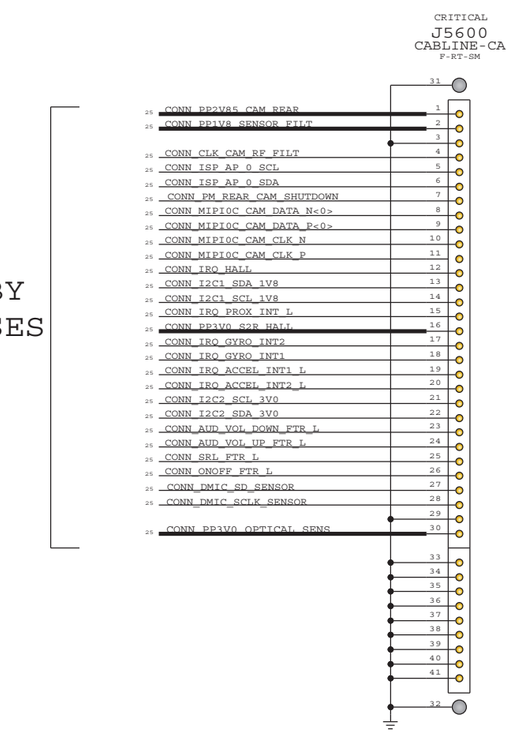
DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
PAGE 55 OF 106
SHEET 26 OF 42

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



CONNECTED BY
PG 54 ALIASES

SENSOR PANEL CONNECTOR
CABLINE-CA CONNECTOR: 518S0787



SYNC MASTER=MARK B. SYNC DATE=N/A

PAGE TITLE

CONNECTOR: SENSOR PANEL CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

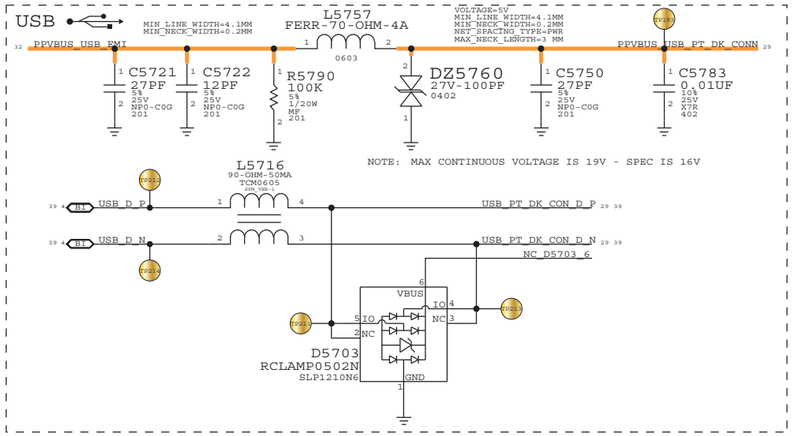
BRANCH

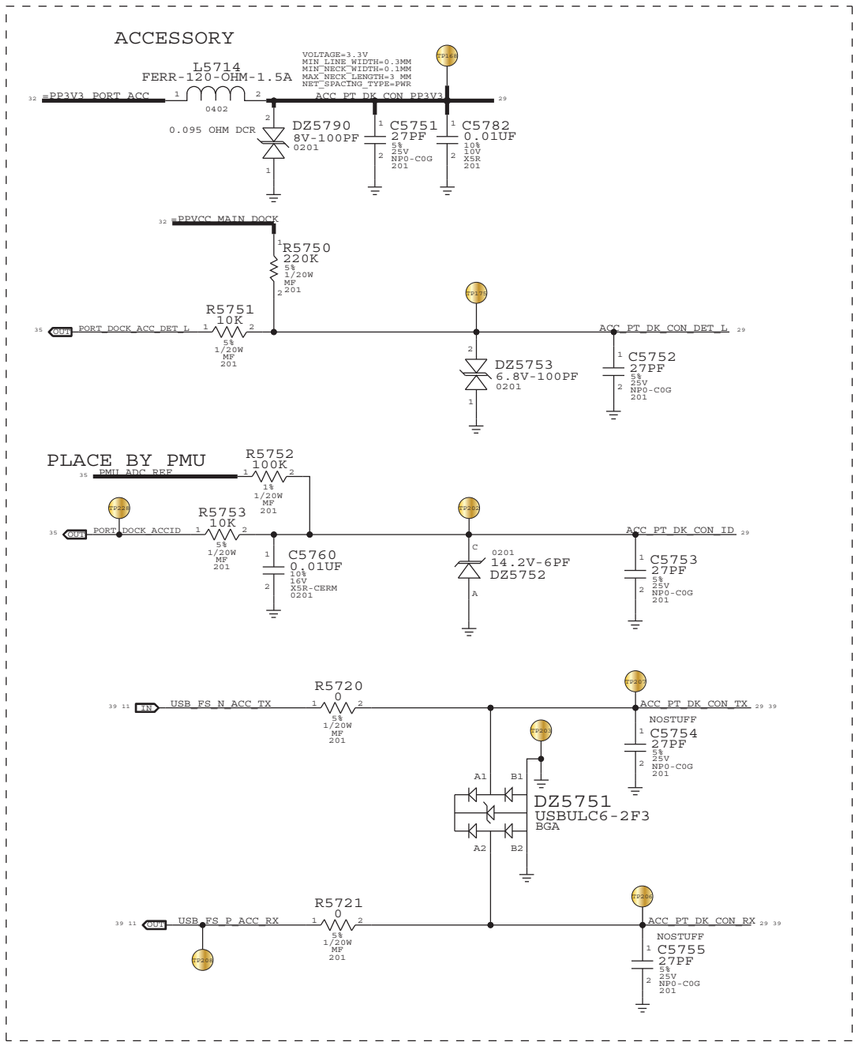
PAGE 56 OF 106

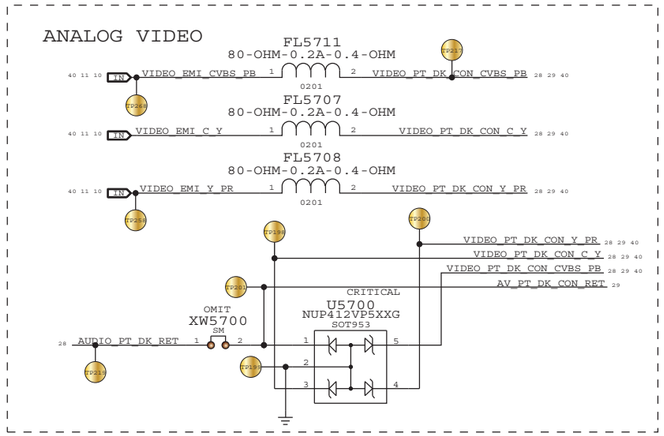
SHEET 27 OF 42

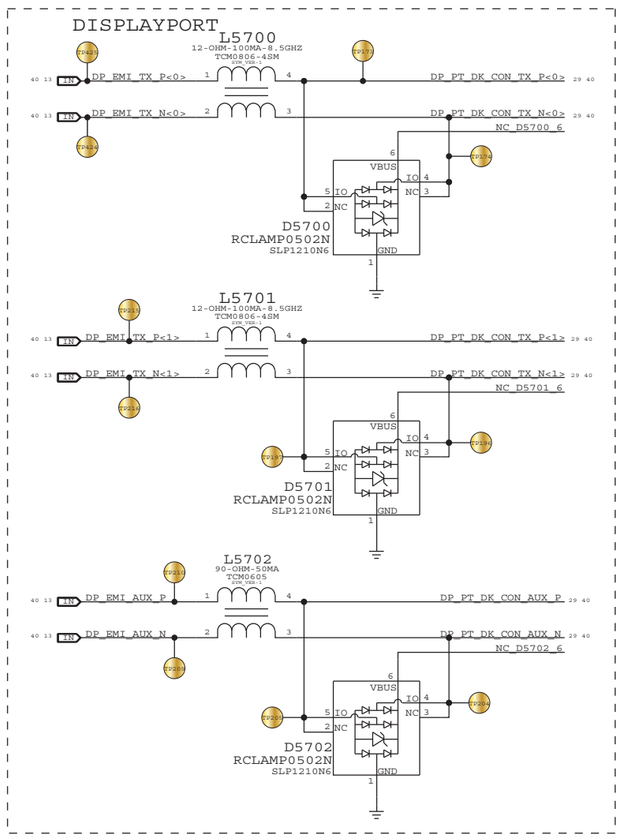
NOTICE OF PROPRIETARY PROPERTY:

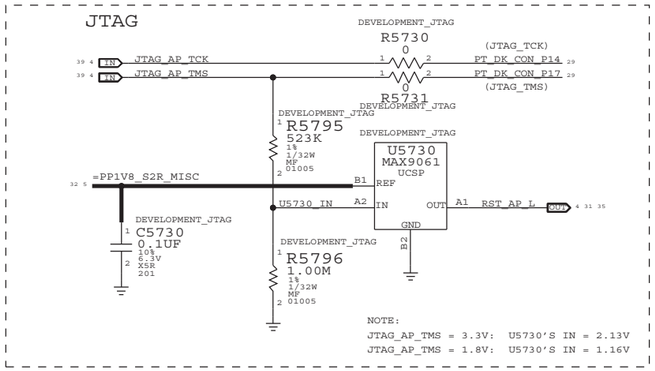
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

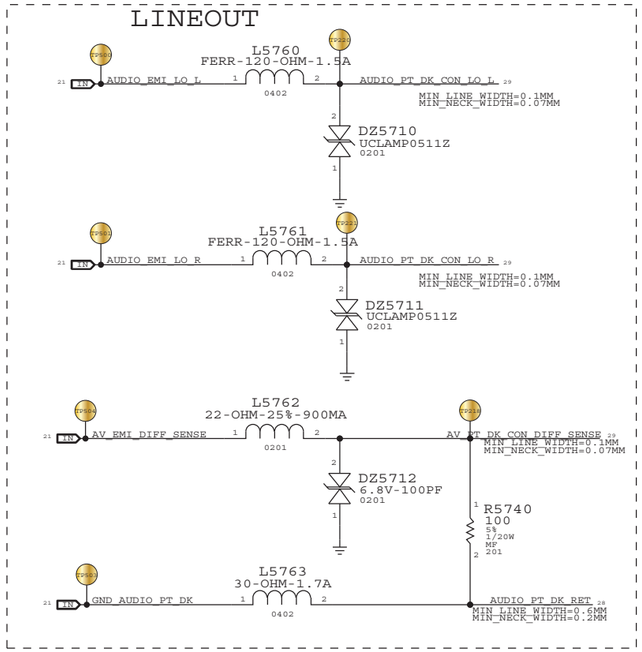


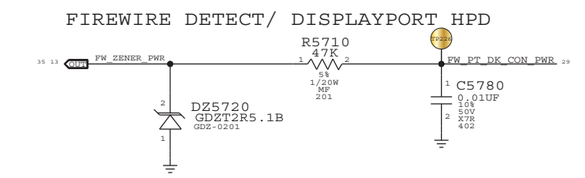












PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0090	377S0081		DZ5751	?
377S0111	377S0099		DZ5710,DZ5711	RADAR:8379541
377S0107	377S0066		DZ5720,DZ5760,DZ5761,DZ5762,DZ5763	RADAR:8289785
155S0625	155S0559		L5700,L5701	RADAR:8423156

SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE

IO FLEX: DOCK COMPONENTS

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

BRANCH

PAGE 57 OF 106

SHEET 28 OF 42

NOTICE OF PROPRIETARY PROPERTY:

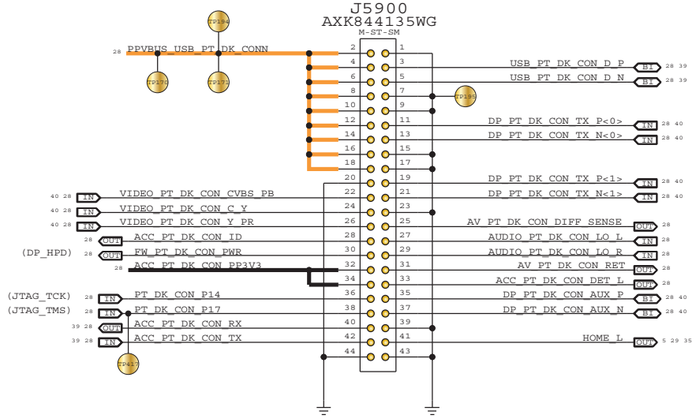
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

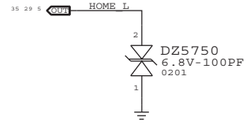
DOCK CONNECTOR

PN 516S0817 (PLUG - MALE)

CRITICAL

J5900
AXK844135WG
M-ST-SM





SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE
IO FELX: B2B Connector

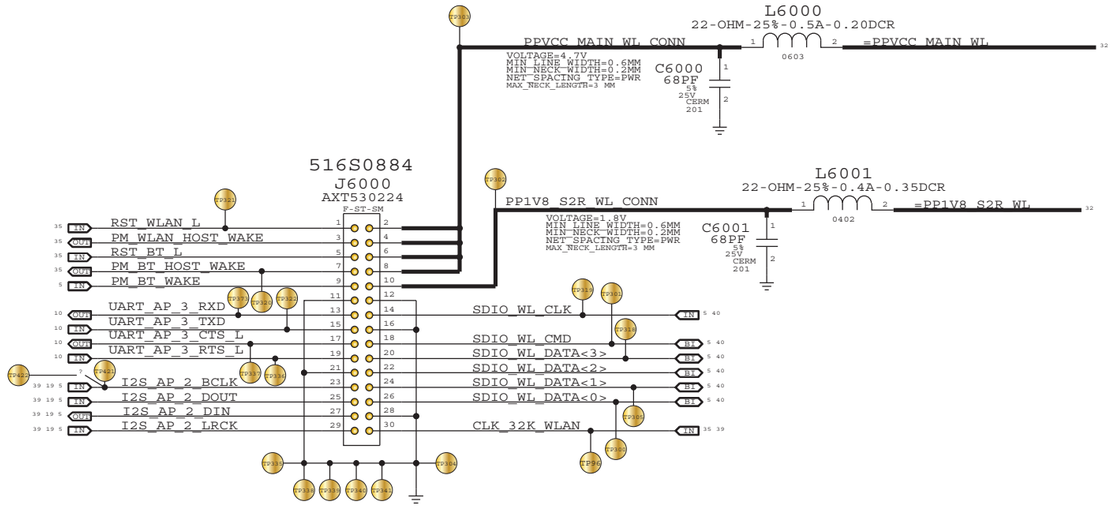
Apple Inc.

DRAWING NUMBER 051-8962
SIZE D
REVISION A.0.0
BRANCH
PAGE 59 OF 106
SHEET 29 OF 42

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

X23 WIFI/BT CONNECTOR



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
CONNECTOR: X23 WIFI/BT

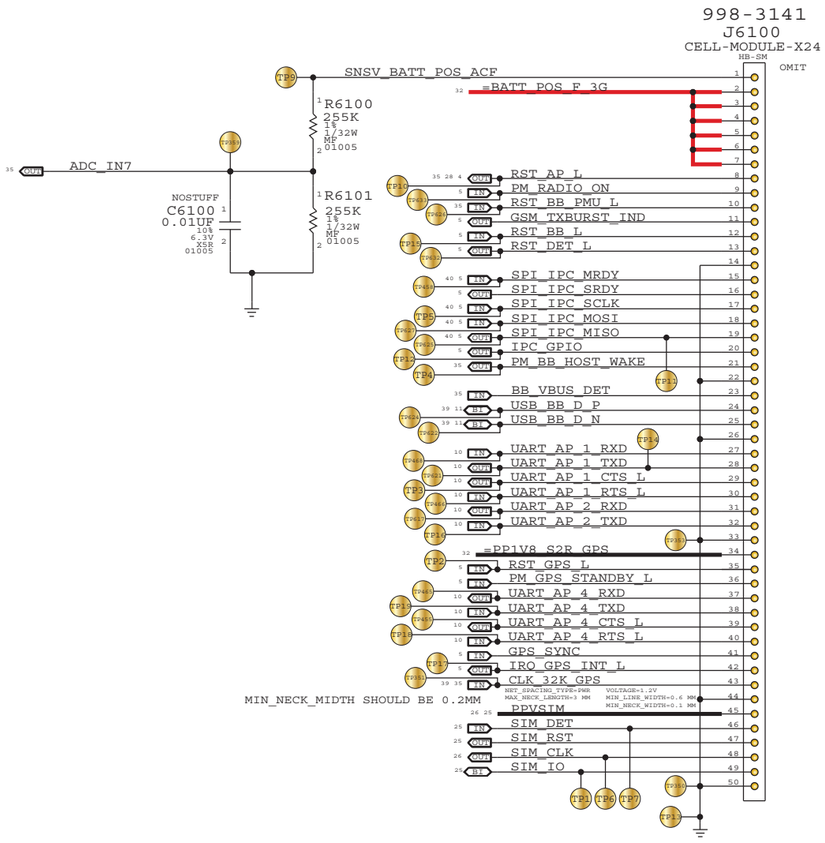
Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
PAGE 60 OF 106
SHEET 30 OF 42

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

X24 CELLULAR/GPS CONNECTOR



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE

CONNECTOR: X24 CELLULAR/GPS

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

BRANCH

PAGE 61 OF 106

SHEET 31 OF 42

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

POWER CONN / ALIAS

LDO RAILS

PROGRAMMABLE ON/OFF

PP3V0_S2R_HALL
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V0_S2R_HALL
= =PP3V0_S2R_HALL_CHSW

PP1V7_VA_VCP
MAKE_BASE=TRUE
VOLTAGE=1.7V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP1V7_VA_VCP

PP3V0_VIDEO
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V0_VIDEO_BUFFER
= =PP3V0_VIDEO_H4

PP3V0_OPTICAL
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V0_OPTICAL

PP3V2_SD
MAKE_BASE=TRUE
VOLTAGE=3.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

PP3V3_ACC
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V3_PORT_ACC

PP3V0_VIDEO_BUF
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V0_VIDEO_BUF

PP3V2_S2R_USBMUX
MAKE_BASE=TRUE
VOLTAGE=3.2V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V2_S2R_USBMUX

PP3V0_IO
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V0_IO_H4
= =PP3V0_IO_MISC

PP2V85_CAM
MAKE_BASE=TRUE
VOLTAGE=2.85V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP2V85_CAM

PP3V0_GRAPE
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V0_GRAPE
= =PP3V0_GRAPE_Z1
= =PP3V0_GRAPE_Z2
= =PP3V0_GRAPE_MARIO1

PP1V1
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
= =PP1V1_PLL_H4
= =PP1V1_MIPI_H4
= =PP1V1_DPORT_H4
= =PP1V1_USB_H4
= =PP1V1_MIPI_PLL_H4
MIN_NECK_MIDTH SHOULD BE 0.2MM

PP1V8_ALWAYS
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP1V8_ALWAYS

BUCK RAILS

PP1V2_SOC
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
= =PPVDD_SOC_H4

PP1V2_CPU
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
= =PPVDD_CPU_H4

PP1V2_S2R
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
= =PP1V2_S2R_H4

PP1V8_S2R
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP1V8_S2R_H4
= =PP1V8_S2R_WL
= =PP1V8_S2R_GPS
= =PP1V8_S2R_MISC

PP1V8
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
= =PP1V8_CAM
= =PP1V8_SENSOR
= =PP1V8_AUDIO
= =PP1V8_H4
= =PP1V8_VDDIO18_H4
= =PP1V8_MIPI_H4
= =PP1V8_DPORT_H4

PP3V3_OUT
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
= =PP3V3_NAND
= =PP3V3_USB_H4
= =PP3V3_MLC_HI
= =PP3V3_LCD
= =PP3V3_NAND_H4

PPLED_OUT
MAKE_BASE=TRUE
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PPLED_REG

PP3V3_MLC_OUT
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V3_MLC

PP1V2
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
= =PP1V2_VDDQ_H4
= =PP1V2_VDDIOD_H4
= =PP1V2_HSIC_H4

GND
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.10MM
NET_SPACING_TYPE=GND
MAX_NECK_LENGTH=5 MM

CHARGER MAIN

PPVCC_MAIN
MAKE_BASE=TRUE
VOLTAGE=4.7V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=1 MM
= =PPVCC_MAIN_AUDIO
= =PPVCC_MAIN_WL
= =PPVCC_MAIN_DOCK
= =PPVCC_MAIN_LED

BATTERY

PPBATT_VCC
MAKE_BASE=TRUE
VOLTAGE=4.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=1.7 MM
= =BATT_POS_F_3G
= =BATT_POS_CONN

USB POWER INPUT

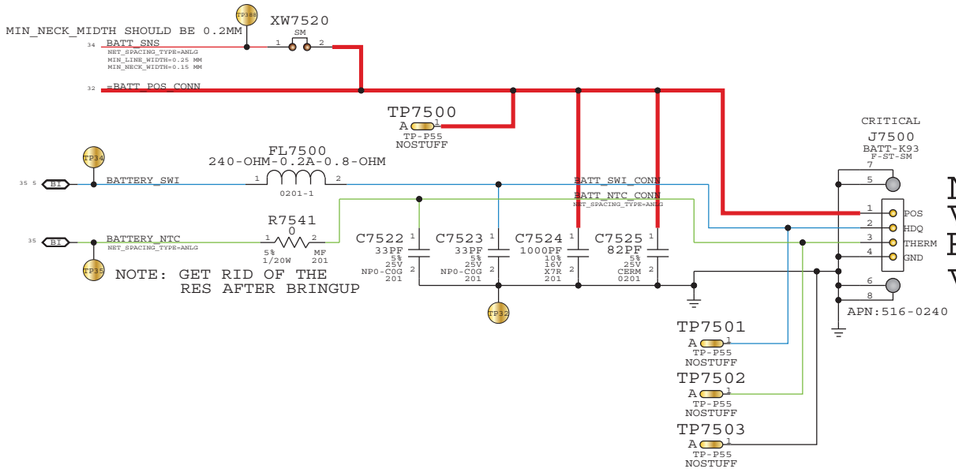
PPVBUS_USB_EMI = PPVBUS_USB_DCIN
MAKE_BASE=TRUE

SYNC_MASTER=YOSH SYNC_DATE=N/A
PAGE TITLE
POWER: ALIASES

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
PAGE 73 OF 106
SHEET 32 OF 42

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



NOTE:
VERIFY PINOUT OF
BATTERY CONNECTOR
VERIFY MOUNTING CONN TO GND

SYNC MASTER=YOSH SYNC DATE=N/A

PAGE TITLE
POWER: BATTERY CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
PAGE 75 OF 106
SHEET 33 OF 42

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0542	1	IC,PMU,ALISON,D1946A2,OTPXX,UFBGA292	U8100	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0392	197S0299		Y8138	ALT FOUNDRY

USB REVERSE VOLTAGE PROTECTION

MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

CRITICAL SHIT
L8112
2.2UH-3.5A-54M-OHM
PIME061E-SM
DCR=54MOHM MAX

This bull shits from APPLE have OMIT manufacturer of the PMIC and not only!

U8100
ALISON-A0-OTPXX
D1946A0-110-00
UFBGA
(SYM 2 OF 3)

CRITICAL
L8100
2.2UH-20%-1.85A-80MOHM
CRITICAL
L8101
2.2UH-20%-1.85A-80MOHM
CRITICAL
L8105
2.2UH-20%-1.85A-80MOHM
CRITICAL
L8107
2.2UH-20%-1.85A-80MOHM
CRITICAL
L8110
2.2UH-20%-1.85A-80MOHM
CRITICAL
L8115
2.2UH-20%-1.85A-80MOHM
CRITICAL
L8119
2.2UH-20%-1.85A-80MOHM
CRITICAL
L8121
2.2UH-20%-1.85A-80MOHM
CRITICAL
L8128
2.2UH-20%-3.3A-0.064OHM
PIME051E-SM
DCR=64MOHM MAX

PST25201B-SM

XW8103 XW8113 XW8117 XW8126 XW8132
SM
NOSTUFF

ADDITIONAL DISTRIBUTED
25UF (NO DE-RATING)

ADDITIONAL DISTRIBUTED
30UF (NO DE-RATING)

ADDITIONAL DISTRIBUTED
14UF (NO DE-RATING)

ADDITIONAL DISTRIBUTED
20UF (NO DE-RATING)

ADDITIONAL DISTRIBUTED
47UF (NO DE-RATING)

ADDITIONAL DISTRIBUTED:
PP1V2: 30UF (NO DE-RATING)
PP1V8: 6UF (NO DE-RATING)

TP8133
TP-P55
NOSTUFF

TP8101
TP-P55
NOSTUFF

CRITICAL
Q8104
FDMC6683
MLP3.3X3.3
RDSON=0.0136@VGS=-2.5V
ID=12.0A

CRITICAL
D8100
SOD-123W
PMEG4030ER

CRITICAL
Q8123
FDMC6676BZ
MLP3.3X3.3

DZ8120
BZT52C10LP
LLP
CRITICAL
NOTE: 10V ZENER

R8116
470K
1%
1/20W
MF
201

R8130
220K
1%
1/20W
MF
201

C8124
2.2UF
10%
25V
X5R-CERM
805

C8125
10UF
10%
25V
X5R
805
CRITICAL
LAYOUT NOTE: PLACE RIGHT AT THE PIN

XW8114
SHORT-0201
NOSTUFF

PPVBUS_PROT
PPVBUS_USB_DCIN
VBUS_PROT_G
PPBATT_VCC
ACT_DIO
NC_CHGB
BATT_SNS
NC_VBUS_A_OV_N
NC_VBUS_B_OV_N
PMU_VCENTER

CHG_A_LX
CHG_B_LX
VBAT
IBAT_S
IBAT
ACT_DIO
VCENTER_A
VBUS_A
VBUS_A_OV_N
VCENTER_B
VBUS_B
VBUS_B_OV_N

VDD_BUCK0
VDD_BUCK2
VDD_BUCK3
VDD_BUCK4
VDD_BUCK5
VDD_BUCK5_BYP
VCC_MAIN_S
VCC_MAIN
VDD_LDO1_6
VDD_LDO2
VDD_LDO3_5_8
VDD_LDO4_7
VDD_LDO9
VDD_LDO10
VDD_LDO11
VDD_LDO12
XTAL1
XTAL2

BUCK0_LXL
BUCK0_LXM
BUCK0_FB
BUCK2_LXL
BUCK2_LXM
BUCK2_LXR
BUCK2_FB
BUCK3_LX
BUCK3_FB
BUCK4_LXL
BUCK4_LXM
BUCK4_FB
BUCK5_LX
BUCK5_BYP
BUCK5_FB

(BYPASS RON=0.14 OHM MAX)

VLDO1 (150MA; 2.5-3.5V) PP3V0_GRAPE
VLDO2 (100MA; 1.65-1.805V; BUCK3) PP1V7_VA_VCP
VLDO3 (50MA; 2.5-3.3V) PP3V0_VIDEO
VLDO4 (100MA; 1.8-3.3V) PP3V0_OPTICAL
VLDO5 (300MA; 2.5-3.6V) PP3V2_SD
VLDO6 (150MA; 2.5-3.6V) PP3V3_ACC
VLDO7 (50MA; 1.5-3.3V) PP3V0_VIDEO_BUF
VLDO8 (10MA; 2.0-3.55V) PP3V2_S2R_USBMUX
VLDO9 (300MA; 1.2-3.0V) PP3V0_IO
VLDO10 (200MA; 2.5-3.55V) PP3V0_S2R_HALL
VLDO11 (200MA; 1.7-3.0V) PP2V85_CAM
VLDO12 (150MA; 0.6-1.3V) PP1V1
ON_BUF PP1V8_ALWAYS

VBUCK4 CPU1V2_SW DSP_SW VBUCK3 CPU1V8_SW WDIG_SW
CPU1V2_SW (RON=0.1 OHM MAX)
DSP_SW (RON=1 OHM MAX)
CPU1V8_SW (RON=0.2 OHM MAX)
WDIG_SW (RON=0.5 OHM MAX)
VBUCK0_SW0_G NC_PMU_VBUCK0_SW0_G
VBUCK0_SW0_S NC_PMU_VBUCK0_SW0_S
VPUMP PMU_VPUMP

C8137
0.01UF
10%
6.3V
X5R
01005

USB/BAT
BUCK
LDO
VCC-MAIN
SWITCH POWER
LDO INPUT
XTAL

NOTE: FOR NO BATTERY SITUATION

PPBATT_VCC
C8100 22UF 20% 6.3V X5R-CERM 603
C8101 22UF 20% 6.3V X5R-CERM 603
R8100 0.5 1% 1/16W MF 402
BATT_POS_RC
MIN_LINE_WIDTH=0.10MM
MIN_NECK_WIDTH=0.20MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
VOLTAGE=4.6V

PP1V8_S2R
C8135 1UF 10% 6.3V CERM 402
PPVCC_MAIN
PP1V2_S2R
C8136 1UF 10% 6.3V CERM 402

NET_SPACING_TYPE=CRYSTAL
CRITICAL
Y8138
32.768K-20PPM-12.5PF
PMU_XTAL PMU_EXTAL
2012
C8142 18PF 5% 25V NP0-C0G 201
C8143 18PF 5% 25V NP0-C0G 201

LDO BYPASS

PP3V0_GRAPE
PP1V7_VA_VCP
PP3V0_VIDEO
PP3V0_OPTICAL
PP3V2_SD
PP3V3_ACC
PP3V0_VIDEO_BUF
C8150 2.2UF 10% 6.3V X5R 402
C8149 2.2UF 10% 6.3V X5R 402
C8148 4.7UF 20% 6.3V X5R-CERM1 402
C8146 2.2UF 10% 6.3V X5R 402
C8145 2.2UF 10% 6.3V X5R 402
C8144 10UF 20% 6.3V CERM-X5R 0402
C8147 2.2UF 10% 6.3V X5R 402

PP3V2_S2R_USBMUX
PP3V0_IO
PP3V0_S2R_HALL
PP2V85_CAM
PP1V1
PP1V8_ALWAYS
C8169 0.22UF 20% 6.3V X5R 0201
C8168 2.2UF 10% 6.3V X5R 402
C8167 2.2UF 10% 6.3V X5R 402
C8153 2.2UF 10% 6.3V X5R 402
C8152 4.7UF 20% 6.3V X5R-CERM1 402
C8151 1UF 10% 6.3V CERM 402

VCC_MAIN BYPASS
TOTAL CAPS = ~400UF
(DISTRIBUTED AND NO DE-RATING)

(PLACE ONE 1UF CAP AT EACH VDD INPUT)

PLACEMENT_NOTE=PLACE NEAR L8225.1
PPVCC_MAIN
C8166 150UF-0.035OHM 20% 6.3V POLY-TANT CASE-B15G-SM
C8165 150UF-0.035OHM 20% 6.3V POLY-TANT CASE-B15G-SM
C8154 10UF 20% 6.3V X5R 603
C8155 10UF 20% 6.3V X5R 603
C8156 4.7UF 20% 6.3V X5R-CERM1 402
C8157 4.7UF 20% 6.3V X5R-CERM1 402
C8158 4.7UF 20% 6.3V X5R-CERM1 402
C8159 4.7UF 20% 6.3V X5R-CERM1 402
C8160 4.7UF 20% 6.3V X5R-CERM1 402
C8161 4.7UF 20% 6.3V X5R-CERM1 402
C8162 4.7UF 20% 6.3V X5R-CERM1 402
C8130 4.7UF 20% 6.3V X5R-CERM1 402
C8131 1.0UF 20% 6.3V X5R 0201-MUR
C8163 82PF 5% 25V CERM 0201
C8164 18PF 5% 25V NP0-C0G 201

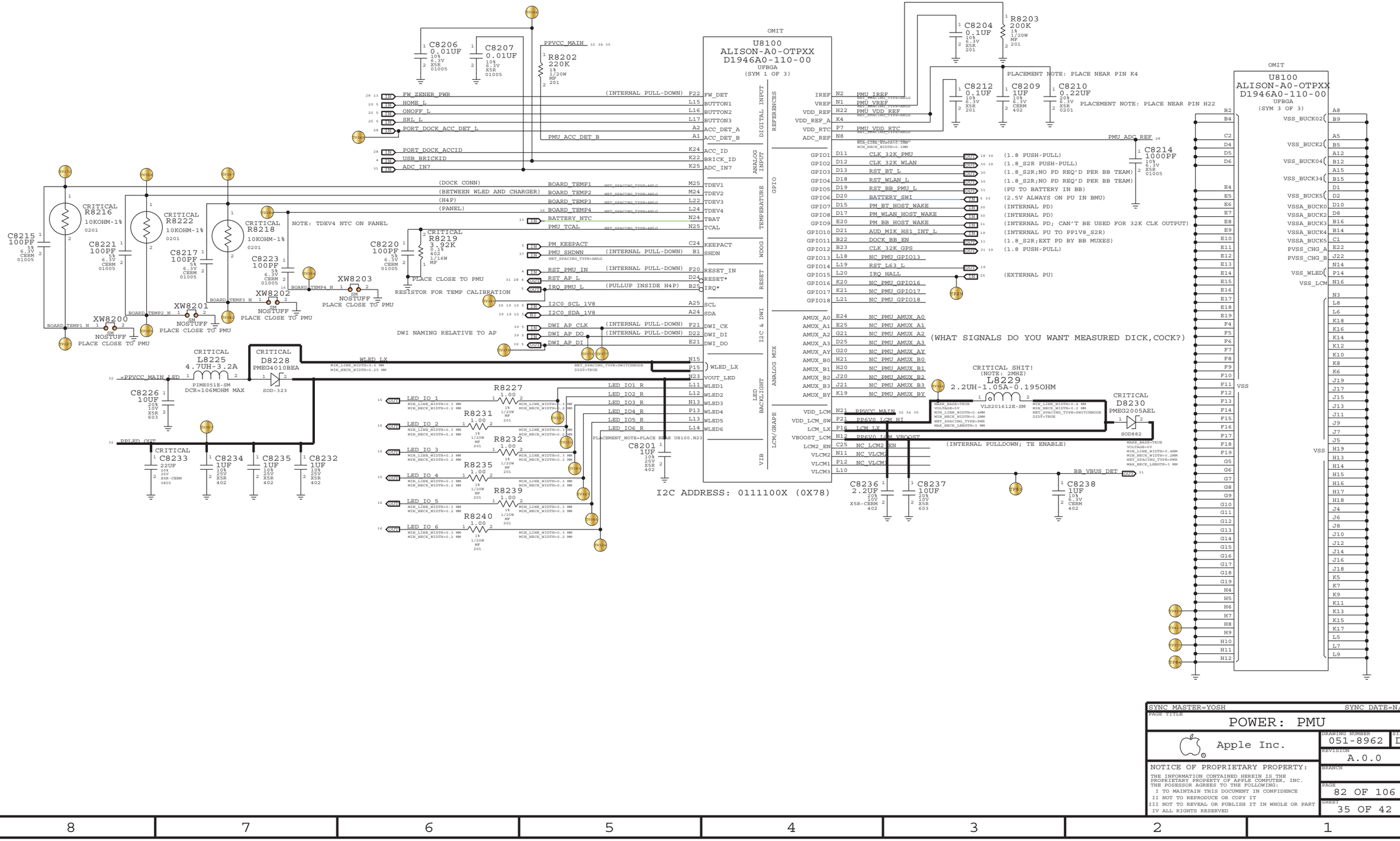
NOTE: CONCERNED ABOUT ESR > 20MOHM

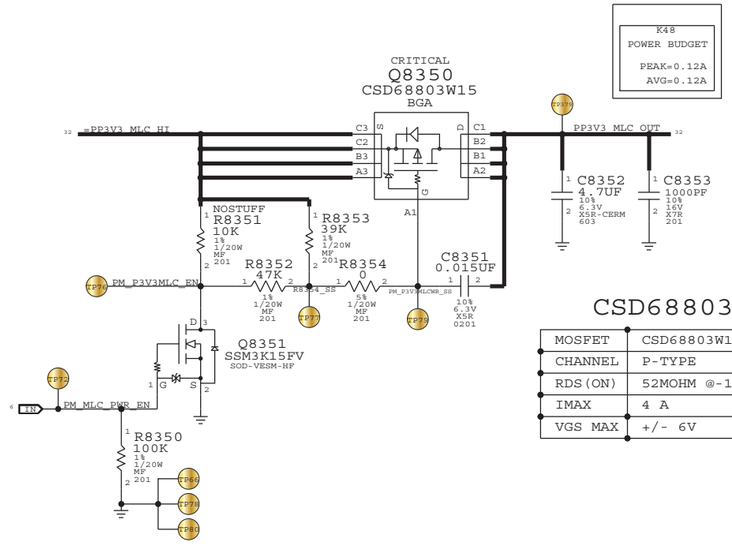
SYNC_MASTER=YOSH SYNC_DATE=N/A
PAGE TITLE
POWER: PMU

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
PAGE 81 OF 106
SHEET 34 OF 42

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


U8100
ALISON-A0-OTPXX
D1946A0-110-00
UFBGA
(SYM 1 OF 3)
OMIT
U8100
ALISON-A0-OTPXX
D1946A0-110-00
UFBGA
(SYM 3 OF 3)
OMIT
DIGITAL INPUT
ANALOG INPUT
TEMPERATURE
WDOG
RESET
I2C & DWI
ANALOG MUX
LED BACKLIGHT
VIB
LCM/GRAPE
REFERENCES
GPIO
VSS
FW_ZENER_PWR
HOME_L
ONOFF_L
SRL_L
PORT_DOCK_ACC_DET_L
PORT_DOCK_ACCID
USB_BRICKID
ADC_IN7
PMU_ACC_DET_B
BOARD_TEMP1
BOARD_TEMP2
BOARD_TEMP3
BOARD_TEMP4
BATTERY_NTC
PMU_TCAL
PM_KEEPACT
PMU_SHDWN
RST_PMU_IN
RST_AP_L
IRQ_PMU_L
I2C0_SCL_1V8
I2C0_SDA_1V8
DWI_AP_CLK
DWI_AP_DO
DWI_AP_DI
WLED_LX
VOUT_LED
WLED1
WLED2
WLED3
WLED4
WLED5
WLED6
LED_IO1_R
LED_IO2_R
LED_IO3_R
LED_IO4_R
LED_IO5_R
LED_IO6_R
PPVCC_MAIN
PPBLED_OUT
=PPVCC_MAIN_LED
PMU_IREF
PMU_VREF
PMU_VDD_REF
PMU_VDD_RTC
PMU_ADC_REF
GPIO1 CLK_32K_PMU (1.8 PUSH-PULL)
GPIO2 CLK_32K_WLAN (1.8_S2R PUSH-PULL)
GPIO3 RST_BT_L (1.8_S2R;NO PD REQ'D PER BB TEAM)
GPIO4 RST_WLAN_L (1.8_S2R;NO PD REQ'D PER BB TEAM)
GPIO5 RST_BB_PMU_L (PU TO BATTERY IN BB)
GPIO6 BATTERY_SWI (2.5V ALWAYS ON PU IN BMU)
GPIO7 PM_BT_HOST_WAKE (INTERNAL PD)
GPIO8 PM_WLAN_HOST_WAKE (INTERNAL PD)
GPIO9 PM_BB_HOST_WAKE (INTERNAL PD; CAN'T BE USED FOR 32K CLK OUTPUT)
GPIO10 AUD_MIK_HS1_INT_L (INTERNAL PU TO PP1V8_S2R)
GPIO11 DOCK_BB_EN (1.8_S2R;EXT PD BY BB MUXES)
GPIO12 CLK_32K_GPS (1.8 PUSH-PULL)
GPIO13 NC_PMU_GPIO13
GPIO14 RST_L63_L
GPIO15 IRQ_HALL (EXTERNAL PU)
GPIO16 NC_PMU_GPIO16
GPIO17 NC_PMU_GPIO17
GPIO18 NC_PMU_GPIO18
AMUX_A0 NC_PMU_AMUX_A0
AMUX_A1 NC_PMU_AMUX_A1
AMUX_A2 NC_PMU_AMUX_A2
AMUX_A3 NC_PMU_AMUX_A3
AMUX_AY NC_PMU_AMUX_AY
AMUX_B0 NC_PMU_AMUX_B0
AMUX_B1 NC_PMU_AMUX_B1
AMUX_B2 NC_PMU_AMUX_B2
AMUX_B3 NC_PMU_AMUX_B3
AMUX_BY NC_PMU_AMUX_BY
VDD_LCM PPVCC_MAIN
VDD_LCM_SW PP6V0_LCM_HI
LCM_LX
VBOOST_LCM PP6V0_LCM_VBOOST
LCM2_EN NC_LCM2_EN
VLCM2 NC_VLCM2
VLCM1 NC_VLCM1
VLCM3
BB_VBUS_DET
C8206 0.01UF 10% 6.3V X5R 01005
C8207 0.01UF 10% 6.3V X5R 01005
R8202 220K 1% 1/20W MF 201
C8204 0.1UF 10% 6.3V X5R 201
R8203 200K 1% 1/20W MF 201
C8212 0.1UF 10% 6.3V X5R 201
C8209 1UF 10% 6.3V CERM 402
C8210 0.22UF 20% 6.3V X5R 0201
C8214 1000PF 10% 6.3V X5R 01005
PLACEMENT NOTE: PLACE NEAR PIN K4
PLACEMENT NOTE: PLACE NEAR PIN H22
(WHAT SIGNALS DO YOU WANT MEASURED DICK,COCK?)
CRITICAL SHIT!
(NOTE: 2MHZ)
L8229
2.2UH-1.05A-0.195OHM
VLS201612E-SM
CRITICAL
D8230
PMEG2005AEL
SOD882
(INTERNAL PULLDOWN; TE ENABLE)
C8236 2.2UF 20% 10V X5R-CERM 402
C8237 10UF 20% 10V X5R 603
C8238 1UF 10% 6.3V CERM 402
C8215 100PF 5% 6.3V CERM 01005
C8221 100PF 5% 6.3V CERM 01005
C8217 100PF 5% 6.3V CERM 01005
C8223 100PF 5% 6.3V CERM 01005
C8220 100PF 5% 6.3V CERM 01005
CRITICAL R8216 10KOHM-1% 0201
CRITICAL R8222 10KOHM-1% 0201
CRITICAL R8218 10KOHM-1% 0201
CRITICAL R8219 3.92K 0.1% 402 1/16W MF
NOTE: TDEV4 NTC ON PANEL
(DOCK CONN)
(BETWEEN WLED AND CHARGER)
(H4P)
(PANEL)
PLACE CLOSE TO PMU
RESISTOR FOR TEMP CALIBRATION
XW8200 SM NOSTUFF PLACE CLOSE TO PMU
XW8201 SM NOSTUFF PLACE CLOSE TO PMU
XW8202 SM NOSTUFF PLACE CLOSE TO PMU
XW8203 SM NOSTUFF PLACE CLOSE TO PMU
DWI NAMING RELATIVE TO AP
CRITICAL L8225 4.7UH-3.2A PIME051E-SM DCR=106MOHM MAX
CRITICAL D8228 PMEG4010BEA SOD-323
C8226 10UF 20% 10V X5R 603
CRITICAL C8233 22UF 20% 25V X5R-CERM 0805
C8234 1UF 10% 25V X5R 402
C8235 1UF 10% 25V X5R 402
C8232 1UF 10% 25V X5R 402
R8227 1.00 1% 1/20W MF 201
R8231 1.00 1% 1/20W MF 201
R8232 1.00 1% 1/20W MF 201
R8235 1.00 1% 1/20W MF 201
R8239 1.00 1% 1/20W MF 201
R8240 1.00 1% 1/20W MF 201
C8201 1UF 10% 25V X5R 402
PLACEMENT_NOTE-PLACE NEAR U8100.N23
I2C ADDRESS: 0111100X (0X78)
SYNC_MASTER=YOSH
SYNC_DATE=N/A
PAGE TITLE
POWER: PMU
Apple Inc.
DRAWING NUMBER 051-8962
SIZE D
REVISION A.0.0
BRANCH
PAGE 82 OF 106
SHEET 35 OF 42
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



CSD68803

MOSFET	CSD68803W15
CHANNEL	P-TYPE
RDS(ON)	52MOHM @-1.8V
IMAX	4 A
VGS MAX	+/- 6V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0972	376S0612		Q8351	RADAR:8537160

SYNC MASTER=YOSH SYNC DATE=N/A

PAGE TITLE
POWER: 3.3V MLC & 1.2V VR

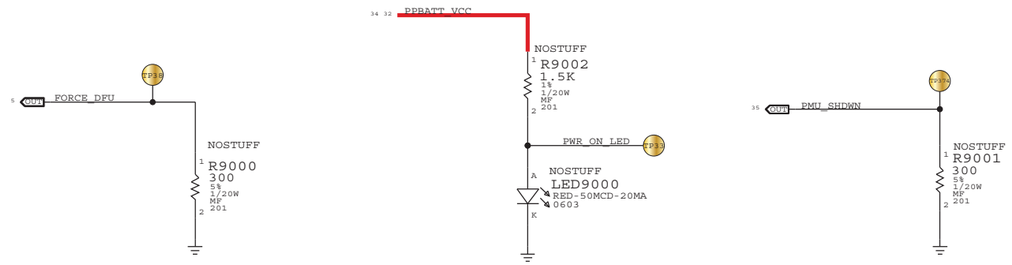
Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
PAGE 83 OF 106
SHEET 36 OF 42

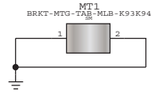
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DEBUG RESET ACCESS

PLACE OUTSIDE OF CAN?



LEFT AND RIGHT MOUNTING TABS



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE: DEBUG AND MISC

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 90 OF 106

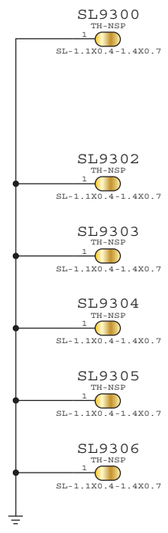
SHEET: 37 OF 42

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
FCT/ICT TEST/BRACKETS

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
PAGE 93 OF 106
SHEET 38 OF 42

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
J63	CLK_50S	CLK	CLK_32K_PMU
J162	CLK_50S	CLK	CLK_32K_WLAN
J161	CLK_50S	CLK	CLK_32K_GPS
J188	CLK_50S	CLK	CLK_CAM_FF
J180	CLK_50S	CLK	CLK_CAM_FF_FILT
J195	CLK_50S	CLK	CLK_CAM_FF_CONN
J196	CLK_50S	CLK	CLK_CAM_RF
J194	CLK_50S	CLK	CLK_CAM_RF_FILT
J130	CLK_50S	CLK	I2S_AP_0_MCK
J132	CLK_50S	CLK	I2S_AP_0_MCK_R
J157	CLK_50S	CLK	CLK_CAM_FF_R
J158	CLK_50S	CLK	CLK_CAM_RF_R

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
J150	NAND_50S	NAND	F0AD<7..0>
J145	NAND_50S	NAND	F0CE0_L
J148	NAND_50S	NAND	F0CE1_L
J147	NAND_50S	NAND	F0CE2_L
J146	NAND_50S	NAND	F0CE3_L
J142	NAND_50S	NAND	F0CE4_L
J164	NAND_50S	NAND	F0CE5_L
J140	NAND_50S	NAND	F0CE6_L
J165	NAND_50S	NAND	F0CE7_L
J141	NAND_50S	NAND	F0CLE
J182	NAND_50S	NAND	F0ALE
J143	NAND_50S	NAND	F0RE_L
J144	NAND_50S	NAND	F0WE_L
J137	NAND_50S	NAND	F0WP_L
J149	NAND_50S	NAND	F1AD<7..0>
J151	NAND_50S	NAND	F1CE0_L
J152	NAND_50S	NAND	F1CE1_L
J153	NAND_50S	NAND	F1CE2_L
J154	NAND_50S	NAND	F1CE3_L
J167	NAND_50S	NAND	F1CE4_L
J160	NAND_50S	NAND	F1CE5_L
J163	NAND_50S	NAND	F1CE6_L
J170	NAND_50S	NAND	F1CE7_L
J155	NAND_50S	NAND	F1CLE
J156	NAND_50S	NAND	F1ALE
J172	NAND_50S	NAND	F1RE_L
J138	NAND_50S	NAND	F1WE_L
J159	NAND_50S	NAND	F1WP_L
J100	NAND_50S	NAND	F2AD<7..0>
J102	NAND_50S	NAND	F2CE0_L
J106	NAND_50S	NAND	F2CE1_L
J108	NAND_50S	NAND	F2CE2_L
J107	NAND_50S	NAND	F2CE3_L
J109	NAND_50S	NAND	F2CLE
J110	NAND_50S	NAND	F2ALE
J111	NAND_50S	NAND	F2RE_L
J131	NAND_50S	NAND	F2WE_L
J133	NAND_50S	NAND	F2WP_L
J114	NAND_50S	NAND	F3AD<7..0>
J115	NAND_50S	NAND	F3CE0_L
J116	NAND_50S	NAND	F3CE1_L
J117	NAND_50S	NAND	F3CE2_L
J118	NAND_50S	NAND	F3CE3_L
J119	NAND_50S	NAND	F3CLE
J120	NAND_50S	NAND	F3ALE
J121	NAND_50S	NAND	F3RE_L
J122	NAND_50S	NAND	F3WE_L
J123	NAND_50S	NAND	F3WP_L

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
H16		JTAG	JTAG_AP_TCK
H15		JTAG	JTAG_AP_TMS
H14		JTAG	JTAG_AP_TDI
H13		JTAG	JTAG_AP_TDO
H20		JTAG	JTAG_AP_TRST_L

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
J1	I2C_50S	I2C	I2C1_SDA_1V8
J2	I2C_50S	I2C	I2C1_SCL_1V8
J3	I2C_50S	I2C	I2C0_SDA_1V8
J4	I2C_50S	I2C	I2C0_SCL_1V8
J91	I2C_50S	I2C	I2C2_SDA_3V0
J92	I2C_50S	I2C	I2C2_SCL_3V0
J98	I2C_50S	I2C	ISP_AP_0_SCL
J99	I2C_50S	I2C	ISP_AP_0_SDA
J100	I2C_50S	I2C	ISP_AP_1_SCL
J101	I2C_50S	I2C	ISP_AP_1_SDA
J103	I2C_50S	I2C	I2C2_SCL_3V0_ALS
J104	I2C_50S	I2C	I2C2_SDA_3V0_ALS
J124	I2C_50S	I2C	ISP_CAM_1_SCL
J125	I2C_50S	I2C	ISP_CAM_1_SDA

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
J92		CRYSTAL	XTAL_24M_I
J90		CRYSTAL	XTAL_24M_O
J93		CRYSTAL	24M_O

VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
J133		VREF	PPVREF_DDR0_CA
J131		VREF	PPVREF_DDR0_DQ
J135		VREF	PPVREF_DDR1_CA
J137		VREF	PPVREF_DDR1_DQ

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
J5	USB_90D	USB	USB_D_P
J6	USB_90D	USB	USB_D_N
J7	USB_90D	USB	USB_PT_DK_CON_D_P
J8	USB_90D	USB	USB_PT_DK_CON_D_N
J182	USB_90D	USB	USB_BB_D_P
J183	USB_90D	USB	USB_BB_D_N
J184	USB_90D	USB	USB_FS_D_P
J185	USB_90D	USB	USB_FS_D_N
J129	USB_90D	USB	USB_FS_N_ACC_TX
J128	USB_90D	USB	USB_FS_P_ACC_RX
J127	USB_90D	USB	ACC_PT_DK_CON_TX
J126	USB_90D	USB	ACC_PT_DK_CON_RX

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_90S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
J190	I2S_50S	I2S	I2S_AP_0_BCLK
J189	I2S_50S	I2S	I2S_AP_0_LRCK
J187	I2S_50S	I2S	I2S_AP_0_DIN
J186	I2S_50S	I2S	I2S_AP_0_DOUT
J192	I2S_50S	I2S	L63_ASP_SDOUT
J177	I2S_50S	I2S	I2S_AP_2_BCLK
J176	I2S_50S	I2S	I2S_AP_2_LRCK
J174	I2S_50S	I2S	I2S_AP_2_DIN
J175	I2S_50S	I2S	I2S_AP_2_DOUT
J191	I2S_50S	I2S	L63_VSP_SDOUT
J181	I2S_50S	I2S	I2S_AP_3_BCLK
J180	I2S_50S	I2S	I2S_AP_3_LRCK
J178	I2S_50S	I2S	I2S_AP_3_DIN
J179	I2S_50S	I2S	I2S_AP_3_DOUT
J193	I2S_50S	I2S	L63_XSP_SDOUT

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
J198		DWI	DWI_AP_CLK
J197		DWI	DWI_AP_DI
J199		DWI	DWI_AP_DO

SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
CONSTRAINTS: ASSIGNMENTS

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
PAGE 100 OF 106
SHEET 39 OF 42

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

ANALOG VIDEO CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
VID_50S	*	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ANALOG_VIDEO	*	*	5:1_SPACING
ANALOG_VIDEO	ANALOG_VIDEO	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
E213	VID_50S	ANALOG_VIDEO	DAC_AP_OUT1 7 11
E214	VID_50S	ANALOG_VIDEO	DAC_AP_OUT2 7 11
E215	VID_50S	ANALOG_VIDEO	DAC_AP_OUT3 7 11
E216	VID_50S	ANALOG_VIDEO	BUF_C_Y 11
E217	VID_50S	ANALOG_VIDEO	BUF_CVBS_PB 11
E218	VID_50S	ANALOG_VIDEO	BUF_Y_PR 11
E219	VID_50S	ANALOG_VIDEO	VIDEO_EMI_CVBS_PB 10 11 28
E220	VID_50S	ANALOG_VIDEO	VIDEO_EMI_C_Y 10 11 28
E221	VID_50S	ANALOG_VIDEO	VIDEO_EMI_Y_PR 10 11 28
E222	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_CVBS_PB 28 29
E223	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_C_Y 28 29
E224	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_Y_PR 28 29

LVDS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
E236	LVDS_100D	LVDS	LVDS_DATA_P<2..0> 14 16
E237	LVDS_100D	LVDS	LVDS_DATA_N<2..0> 14 16
E238	LVDS_100D	LVDS	LVDS_DATA_CONN_P<2..0> 16
E239	LVDS_100D	LVDS	LVDS_DATA_CONN_N<2..0> 16
E240	LVDS_100D	LVDS	LVDS_CLK_P 14 16
E241	LVDS_100D	LVDS	LVDS_CLK_N 14 16
E242	LVDS_100D	LVDS	LVDS_CLK_CONN_P 16
E243	LVDS_100D	LVDS	LVDS_CLK_CONN_N 16

MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
E91	MIPI_100D	MIPI	MIPID_AP_DATA_P<0> 7 14
E92	MIPI_100D	MIPI	MIPID_AP_DATA_N<0> 7 14
E93	MIPI_100D	MIPI	MIPID_AP_DATA_P<1> 7 14
E94	MIPI_100D	MIPI	MIPID_AP_DATA_N<1> 7 14
E95	MIPI_100D	MIPI	MIPID_AP_DATA_P<2> 7 14
E96	MIPI_100D	MIPI	MIPID_AP_DATA_N<2> 7 14
E97	MIPI_100D	MIPI	MIPID_AP_DATA_P<3> 7 14
E270	MIPI_100D	MIPI	MIPID_AP_DATA_N<3> 7 14
E97	MIPI_100D	MIPI	MIPID_AP_CLK_P 7 14
E98	MIPI_100D	MIPI	MIPID_AP_CLK_N 7 14
E331	MIPI_100D	MIPI	MIPI0C_AP_DATA_P<0> 7 27
E332	MIPI_100D	MIPI	MIPI0C_AP_DATA_N<0> 7 27
E333	MIPI_100D	MIPI	MIPI0C_AP_CLK_P 7 27
E334	MIPI_100D	MIPI	MIPI0C_AP_CLK_N 7 27
E343	MIPI_100D	MIPI	MIPI0C_CAM_DATA_P<0> 25 27
E344	MIPI_100D	MIPI	MIPI0C_CAM_DATA_N<0> 25 27
E345	MIPI_100D	MIPI	MIPI0C_CAM_CLK_P 25 27
E346	MIPI_100D	MIPI	MIPI0C_CAM_CLK_N 25 27
E347	MIPI_100D	MIPI	MIPI1C_AP_DATA_P<0> 7 26
E348	MIPI_100D	MIPI	MIPI1C_AP_DATA_N<0> 7 26
E349	MIPI_100D	MIPI	MIPI1C_AP_CLK_P 7 26
E350	MIPI_100D	MIPI	MIPI1C_AP_CLK_N 7 26
E351	MIPI_100D	MIPI	MIPI1C_CAM_DATA_P<0> 25 26
E352	MIPI_100D	MIPI	MIPI1C_CAM_DATA_N<0> 25 26
E353	MIPI_100D	MIPI	MIPI1C_CAM_CLK_P 25 26
E354	MIPI_100D	MIPI	MIPI1C_CAM_CLK_N 25 26

DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
E249	DP_100D	DP	DP_AP_TX_P<0> 7 10 13
E248	DP_100D	DP	DP_AP_TX_N<0> 7 10 13
E246	DP_100D	DP	DP_AP_TX_P<1> 7 10 13
E250	DP_100D	DP	DP_AP_TX_N<1> 7 10 13
E251	DP_100D	DP	DP_AP_AUX_P 7 13
E252	DP_100D	DP	DP_AP_AUX_N 7 13
E273	DP_100D	DP	DP_EMI_TX_P<0> 13 28
E274	DP_100D	DP	DP_EMI_TX_N<0> 13 28
E275	DP_100D	DP	DP_EMI_TX_P<1> 13 28
E276	DP_100D	DP	DP_EMI_TX_N<1> 13 28
E277	DP_100D	DP	DP_EMI_AUX_P 13 28
E272	DP_100D	DP	DP_EMI_AUX_N 13 28
E327	DP_100D	DP	DP_PT_DK_CON_TX_P<0> 28 29
E326	DP_100D	DP	DP_PT_DK_CON_TX_N<0> 28 29
E328	DP_100D	DP	DP_PT_DK_CON_TX_P<1> 28 29
E331	DP_100D	DP	DP_PT_DK_CON_TX_N<1> 28 29
E330	DP_100D	DP	DP_PT_DK_CON_AUX_P 28 29
E332	DP_100D	DP	DP_PT_DK_CON_AUX_N 28 29

AUDIO/SPEAKER

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIO	*	1:1_DIFFPAIR
SPEAKER	*	SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
E698	AUDIO	AUDIO	LEFT_CH_OUT_P 19 20
E699	AUDIO	AUDIO	LEFT_CH_OUT_REF 19 20
E696	AUDIO	AUDIO	LEFT_CH_P 20
E695	AUDIO	AUDIO	SSM2375_L_IN_P 20
E694	AUDIO	AUDIO	SSM2375_L_IN_N 20
E693	AUDIO	AUDIO	RIGHT_CH_OUT_P 19 20
E692	AUDIO	AUDIO	RIGHT_CH_OUT_REF 19 20
E691	AUDIO	AUDIO	RIGHT_CH_P 20
E690	AUDIO	AUDIO	SSM2375_R_IN_P 20
E689	AUDIO	AUDIO	SSM2375_R_IN_N 20
E572	AUDIO	AUDIO	EXT_MIC_P 19 23
E573	AUDIO	AUDIO	EXT_MIC_REF 19 23

SDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SDIO_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SDIO	*	*	2:1_SPACING
SDIO_CLK	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
E600	SDIO_50S	SDIO_CLK	SDIO_WL_CLK 5 30
E598	SDIO_50S	SDIO_CLK	SDIO_WL_CLK_R
E599	SDIO_50S	SDIO	SDIO_WL_CMD 5 30
E597	SDIO_50S	SDIO	SDIO_WL_DATA<3..0> 5 30

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
E166	SPI_50S	SPI	SPI_GRAPE_MISO 5 17
E164	SPI_50S	SPI	SPI_GRAPE_MOSI 5 17
E163	SPI_50S	SPI	SPI_GRAPE_SCLK 5 17
E162	SPI_50S	SPI	SPI_GRAPE_CS_L 5 17
E165	SPI_50S	SPI	SPI_IPC_MISO 5 31
E161	SPI_50S	SPI	SPI_IPC_MOSI 5 31
E160	SPI_50S	SPI	SPI_IPC_SCLK 5 31
E167	SPI_50S	SPI	SPI_IPC_MRDY 5 31

SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
CONSTRAINTS: ASSIGNMENTS

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
PAGE 101 OF 106
SHEET 40 OF 42

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,BOTTOM	NO_TYPE,BGA,BGA06-06	MM	15.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

SINGLE-ENDED PHYSICAL RULES
45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	ISL2,ISL3,ISL8,ISL9	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL4,ISL5,ISL6,ISL7	Y	0.060 MM	0.060 MM	3.0 MM		
45_OHM_SE	*	N	0.060 MM	0.060 MM	3.0 MM		

50 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	3.0 MM		
50_OHM_SE	*	N	0.050 MM	0.050 MM	3.0 MM		

50 OHMS - CLEAR ON LAYER 2 AND 5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE_RF	TOP	Y	0.240 MM	0.240 MM	3.0 MM		
50_OHM_SE	ISL4	Y	0.060 MM	0.060 MM	3.0 MM		

50 OHMS - CLEAR ON TOP AND BOTTOM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	ISL2,ISL9	Y	0.090 MM	0.090 MM	3.0 MM		

DIFFERENTIAL PAIR PHYSICAL RULES
100 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	TOP,BOTTOM	Y	0.076 MM	0.076 MM		0.210 MM	0.210 MM
100_OHM_DIFF	N	Y	0.057 MM	0.057 MM	=STANDARD	0.300 MM	0.300 MM

90 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.095 MM	0.095 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL3,ISL8,ISL9	Y	0.054 MM	0.054 MM	=STANDARD	0.200 MM	0.100 MM
90_OHM_DIFF	ISL4,ISL5,ISL6,ISL7	Y	0.060 MM	0.060 MM	=STANDARD	0.200 MM	0.100 MM

AUDIO PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.3 MM	0.19MM	10 MM	0.08 MM	0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.08 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.060 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.090 MM	?
2:1_SPACING	*	0.120 MM	?
2.5:1_SPACING	*	0.150 MM	?
3:1_SPACING	*	0.180 MM	?
4:1_SPACING	*	0.240 MM	?
5:1_SPACING	*	0.300 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?

*NOTE: ASSUMING 0.060MM DIELECTRIC THICKNESS

POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	900
GND_P1SPACING	*	0.1 MM	950
SWITCHNODE	*	0.5 MM	1000
SWITCHNODE	TOP,BOTTOM	0.2 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
PWR	*	*	PWR_P1SPACING
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING

NOTES:

0.075 MM ~ 3 MIL
0.089 MM ~ 3.5 MIL
0.102 MM ~ 4 MIL
0.114 MM ~ 4.5 MIL
0.125 MM ~ 5 MIL
0.140 MM ~ 5.5 MIL
0.15 MM ~ 6 MIL
0.18 MM ~ 7 MIL
0.2 MM ~ 8 MIL
0.25 MM ~ 10 MIL
0.3 MM ~ 12 MIL
0.33 MM ~ 13 MIL
0.4 MM ~ 16 MIL
1.0 MM = 39.37 MIL

SYNC MASTER=MIKE SYNC DATE=N/A

PAGE TITLE
CONSTRAINTS: MLB RULES

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
PAGE 102 OF 106
SHEET 41 OF 42

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE

CONSTRAINTS: RF RULES

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

BRANCH

PAGE 106 OF 106

SHEET 42 OF 42

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED